WERSI

TECHNICAL DATA
OMEGA DX 10
and
EX 10 EXPANDER

AM 3174

First Edition

THE DIGITAL SOUND SENSATION

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OMEGA DX 10
and
EX 10 EXPANDER

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I. GOAL

This manual is provided to extend your understanding of the OMEGA DX 10 and EX 10 R MIDI Expander and is provided for the technically interested. Since the DX 10 and EX 10 R are technically similar, and in many cases identical, the text will refer only to EX 10 R but applies to both instruments except where noted.

This manual is not written for the experienced technician as it is for the interested hobbyist. In it we describe the general operation (total picture) of the instrument and the operation of each circuit board.

II. TECHNICAL CONCEPT

A. Conventional Organ Systems

To help you better understand the new DX 10/EX 10 sound synthesizing concepts, let's take a look at the other current synthesizers.

1. Analog Organ

This is the oldest, most widely used type of keyboard. It contains the basic modules VCO, VCA, VCF and envelope curve generators of the type ADSR, LFO and the like. The parameters of all basic modules can be controlled by "analog" voltages. The necessary control voltages are produced by the keyboard, control potentiometers, wheels, the foot pedal and envelope curve generators.

Using this procedure, it is impossible to get a targeted upper harmonic spectrum. Fixed formants are not taken into account at all.

2. Analog Organ with Digital Control

The sound generating principle is the same as for analog synthesizers. Only the keyboard data are acquired digitally and transmitted to the sound generating modules – also digitally (DCO = digital controlled oscillator; DCA, DCF, etc). The advantage to this system is that all parameters can be removed from the memory, and the keyboard is for the most part MIDI-capable.

3. Digital Systems with Digitally Recorded Sound

Digitally recorded sounds are used in musical instruments from synthesizers to rhythm units. While it is a very reliable method where the pitch of the sound is not changing (as in percussion instruments), this method has its drawbacks when used in keyboard instruments.

A trumpet may be digitally recorded at the pitch of middle-A, and playing it at middle-A on the keyboard will produce a very true sound. However, as you move away from the pitch at which the trumpet was recorded (A), the sound will begin to lose its trueness.

B. The Advanced DX System with Full Digital Sound Generation

In this technology by WERSI, all tone colors are calculated by a multi-processor system and transformed into electroacoustic vibrations by digital-analog converters. The processor system consists of:

- a master processor which is responsible for the entire organization and the keyboard and switching;
- a co-processor that calculates and outputs the amplitude curves of all sound production units; and
- up to 20 slave microcomputers which output a wave shape corresponding to the frequency envelope curve. The wave shape is calculated by Fourier synthesis, up to 32 harmonics (upper harmonics) and can be outputted online or as a fixed formant.

For each selected sound, 1 or more sound production units (hereafter called slaves) are supplied with data from the master processor and then start automatically and synchronously with the co-processor, which must provide the volume in each case, with the output of the sound. The advantage of this system is that various sound generating systems are used independently of any special hardware, and several sounds can be outputted simultaneously by the starting of several slaves. Since only the data that is processed determines the sound, sound changes can be continuously fed into the memories without using additional hardware. This is done either via the programming of the unit itself or by external media, such as cartridges.

For users who prefer analog control, the digitally controllable filter was also added (24 dB/oct.). Furthermore, 3 bucket brigades provide effects such as a rotating speaker, chorus or flanging.

As shown by a comparison of the various synthesizer concepts, the advanced DX concept affords the most complex and flexible type of sound generation.

Overall Block Diagram of the DX 10 System

The block diagram in Fig. 1 shows the overall structure of the DX 10 (EX 10 R), divided according to PC boards and functional groups.

The left portion includes the control panels. We distinguish between digital and analog input data. The analog inputs include all slide controls, the wheels, as well as the touch sensors and volume pedal. These analog signals are multiplexed and sent to an A/D converter which provides the analog data in digital form for the main processor.

As digital inputs we have 64 switches which are polled serially in groups of 16.

The keyboard is another input. Since the dynamic interrogation of 49 keys would overload the master processor, a special single-chip microcomputer (Z 8601) does this job, transmitting to the master only key changes, including the key speed, via the data bus.

The digital output includes the latches and the D/A converter on the analog PC board at the top of the diagram. The signals of these units control the analog units VCF, Wersivoice (WV) and the channel selection stages.

As in a conventional microprocessor system, we find the working RAM (working memory) and the program ROM, containing the command program, as well as a serial interface (ACIA) for MIDI in/out.

The sound parameters are in special ROMs and RAMs (voice ROM for 20 DMS sounds, voice RAMs for 10 CVs + 8 presets). Because of the size of the address area, the modules must be banked using a switch together with the addressing of the cartridge.

As mentioned above, the scope of tests for a microprocessor (uP) is too complex, so the function of amplitude envelope control is handled by the co-processor, which receives its program and data via a dual port RAM, which can be simultaneously read

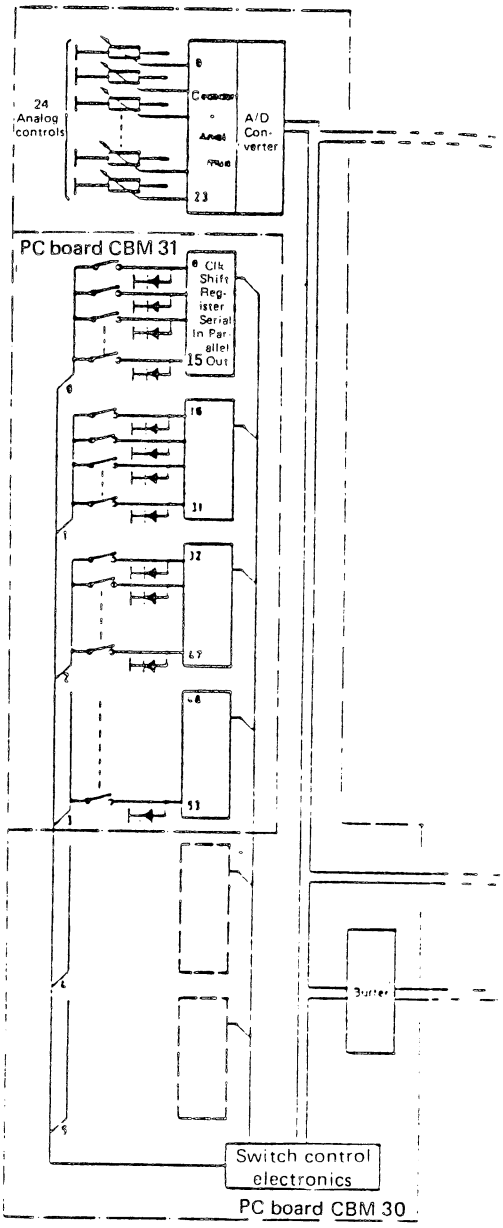
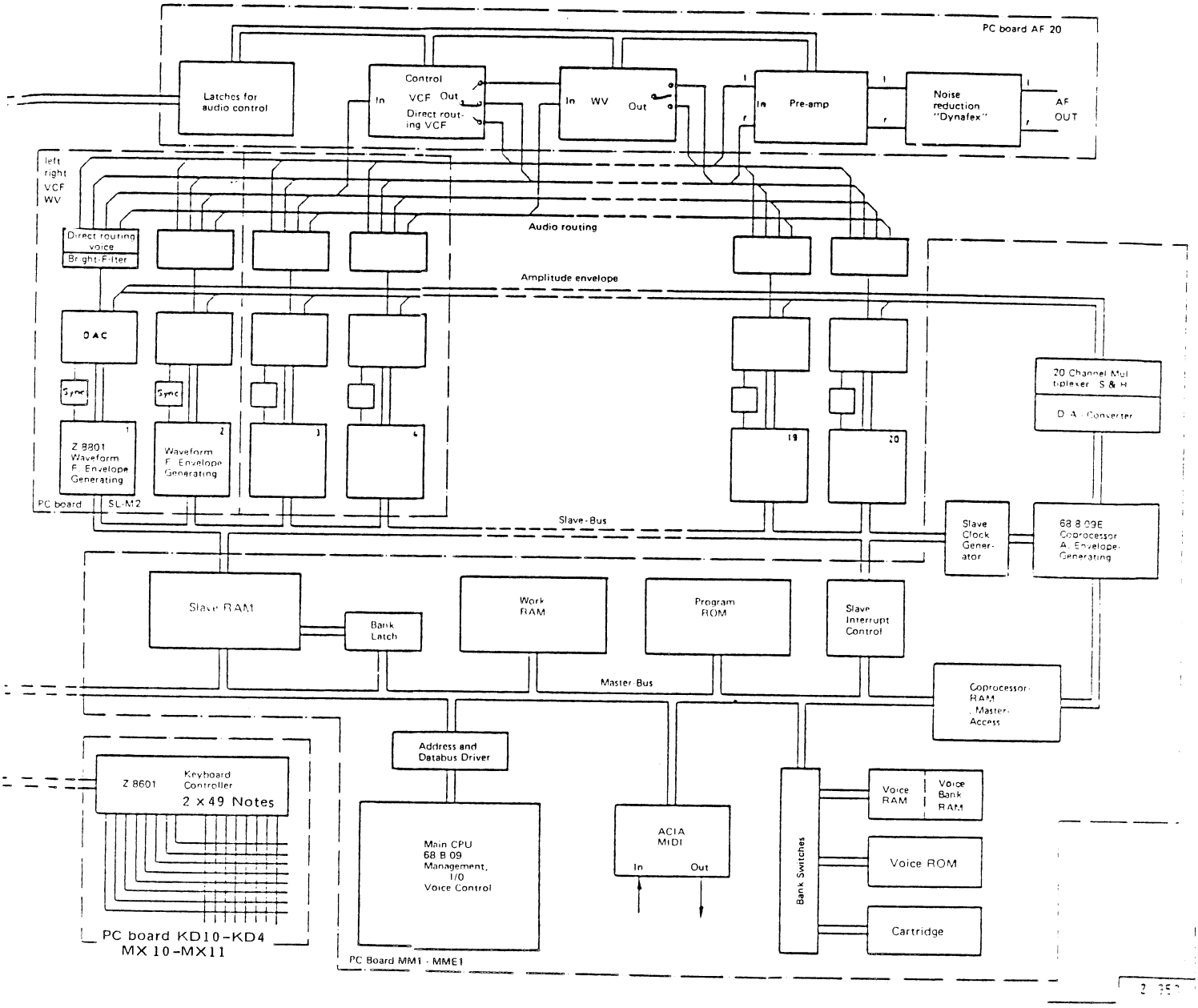


Fig. 1: Overall block-diagram of the DX 10 (EX 10 R) (for the EX 10, KD 10 and KD 4 will not be used and ME 2 will be used in place of CBM 30 and CBM 31).

and written by both the master and the co-processor. It calculates the amplitude data and outputs them via D/A converters, a 20-channel demultiplexer with sample and hold, to the slave DACs in analog form. Additionally, it provides for a synchronous flow of the frequency and amplitude envelope of each slave with the aid of individual clock pulses.



The up to 20 slave processors are single-chip computers like the keyboard controller. They get their data concerning wave shape, frequency envelope, synthesis process and pitch via the slave RAM, which can address different blocks via bank latch 32. A reply of the slaves to the master is given via the slave-interrupt control. These processors then start their wave shape output timer via the DAC. Filter processing is then accomplished, optionally via the bright filter, until the finished audio signal is assigned via the routing switch to the audio buses left, right, VCF and WV. After subsequent processing by VCF and WV, the audio signal travels through the preamp to the noise suppression circuit, and finally to the output jacks.

III. CIRCUIT DIAGRAMS and TECHNICAL DESCRIPTION

This section presents the precise circuit diagrams, arranged according to PC boards, with brief explanations. The component layout is reprinted here – as viewed from both sides of the board, for the control panels.

A. Technical Description of PC Board PS 20

The switching power supply PS 20 operates on the flow transducer principle. This transducer principle makes it possible to generate several controlled output voltages with only a transformer and a choke coil. The efficiency is high and the ripple of the output voltages low.

Fig. 2 shows the circuit diagram of such a transducer; Fig. 3 shows the respective (idealized) voltage and current curves.

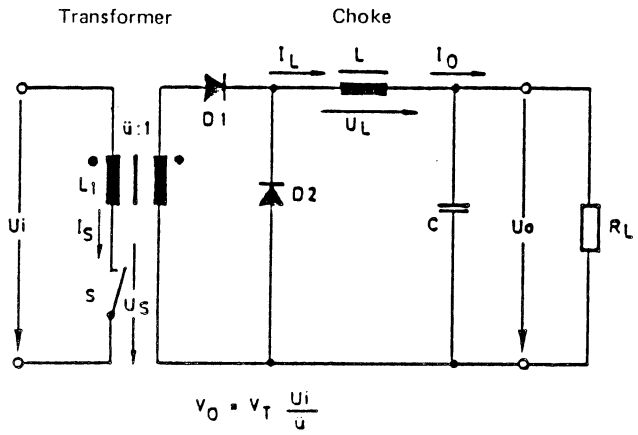
During the make phase t_L (S closed), the diode D1 also conducts current; energy is transferred to the load circuit R_L (hence the name flow transformer). Simultaneously, choke coil L receives energy with the linearly increasing current I_L. Diode D2 is not conducting.

If switch S is open, D1 is polarized in the blocking direction and therefore de-energized. Because of the energy stored in choke coil L, the current proceeds through L and hence through the load circuit in the same direction, the now-conducting diode D2 acting as a freewheeling diode. Since U_0 is approximately constant, the choke current again decreases linearly. C filters the starting voltage U_0. The magnetic energy forcibly absorbed from the transformer during the make phase – represented by the hatched magnitization current component of the switching current I_s – is undesired for the operation of the circuit. It must be absorbed by suitable means, transmitted back to DC source U or otherwise utilized. Thus, the voltage at the transformer or the switch (U_s) is at the same time restricted.

Let us consider the actual circuit of the power supply PS 20. The major components of the circuit are easily identified:

The transformer HFT 1 with the primary winding n1 and the secondary windings n2-n5.

The windings (n1, n2, n3) of choke coil MDR 1 are wound on the same core. This principle permits relatively good regulation of the $\pm$14 V outputs, although only the 5 V output is kept absolutely constant. The



t_L = make phase
t_S = break phase
T = period

V_T = make-to-break ratio = $\frac{T}{t_L}$

Fig. 2: Circuit diagram of a flow transducer.

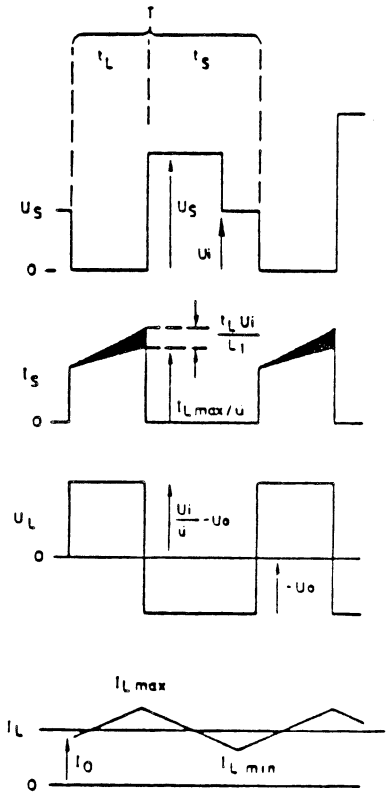


Fig. 3: Voltage and current curves of the transducer.

rectifier diodes D4, 5, 6, 7 are superfast special diodes (to minimize switching losses).

DD1 is a Schottky double diode with low forward voltage.

C1, 2, 3 are switch-proof electrolytic capacitors with excellent high-frequency (HF) properties. The role of the switch is played by a power FET, Q3. There are several reasons why a field effect transistor is used: very good switching speed, low driver power, ruggedness.

The network D 10, R 35, C 17, 18 and R 36, C 16 at the drain of the transistor represents what we called a "suitable means" in the description of the circuit.

The network is dimensioned so that the energy during the break phase is reliably absorbed and the voltage at the drain limited to about 80 V. After the energy has been drained, the drain voltage drops to U_i (Fig. 2, U_S).

Since this energy is stored in the core of the transformer, it is available at each winding, and thus at n3, where, with the aid of D9, we take part of this energy as negative voltage which is available "for free" as an auxiliary voltage (used for the display) at C14 or at the Zener diode chain D6, 5 and 4.

The voltage at n5 is brought out as DC voltage (about 8 V_{SS}).

So much for the transformer, switch and choke coil.

Since we are dealing with a switching power supply and must work with terms such as switching transistor, make phase, make-to-break ratio and control, we must necessarily take the most important part of the circuit under scrutiny: the control unit.

There are various possibilities for keeping the output voltage of a switching power supply constant. We chose the "constant frequency, variable make-to-break ratio" method.

In the PS 20 we are working with the UC 3842, a very modern integrated circuit. In the overall circuit

diagram, the internal structure of the ICs is indicated schematically. We can best understand the function if we "run through" a working cycle.

The oscillator runs at a frequency of about 100 kHz. The positive wave shape sets the flip-flop and hence the drive output; Q3 switches on (make phase). The current I_S now flows in the primary winding of HFT 1, Q3 and R 37 (Fig. 2). The voltage developed across R 37 (which is proportional to the current I_S) is applied to the positive input of the comparator. (The filter R 40, 44, C 19, 22 keeps out interfering high-frequency oscillations). Once this linearly increasing voltage has reached the level at the negative input, the comparator switches, resetting the flip-flop; the drive output goes to 0, Q3 opens, and we are now in the break phase.

The cycle starts over again with the next positive edge of the oscillator. Let us again consider that the current I_S (and hence the voltage at the positive input) rises as a linear function of time and changes of the voltage at the negative input.

If we make this voltage more positive, it will take longer for the linearly increasing voltage to be reached at the other input; the make phase is longer. Accordingly, the make phase becomes shorter if we reduce the voltage. The length of the make phase and hence the make-to-break ratio therefore depends on the voltage at the negative input.

This voltage is provided by the (inverting) AGC (Automatic Gain Control) amplifier, which is also integrated. Its positive input is connected to the internal +2.5 V reference voltage; its negative input is connected via the voltage divider R 26/R 42 to the 5 V output of the power supply. If the voltage at the output decreases (because of an increased load), the amplifier output, that is, the comparator threshold, becomes more positive and the make phase becomes longer. Thus the output voltage rises again to 5 V and the control process is concluded. The entire system also naturally functions in the other direction.

Another feature of the control IC must be mentioned. It exhibits Schmidt trigger behavior relative to its supply voltage (pin 7). The thresholds are about 16/10 V. This means that over 16 V, it functions and below 10 V it "switches itself off."

In Practical Terms This Means That:

After the AC voltage is switched on, we have about +40 V at the charging electrolytic capacitor C 27. At electrolytic capacitor C 26, the voltage rises relatively slowly (R 41 = 10 k); the IC draws a current of about 1 mA. When the 16 V threshold is reached, the IC and hence the entire power supply, starts. The output voltages build up, and a +14 V output then starts to supply the IC via D8 (the IC's consumption is now 6-8 mA). If this takeover does not occur for some reason, the elevated consumption at R 41 causes an increased voltage drop, so the voltage at C 26 drops rapidly below 10 V; the IC switches off again, the consumption drops to 1 mA, and the process repeats itself cyclically.

Current Limitation

The output currents are registered via R 32, R 33, R 34. The respective comparators (IC 2) are correspondingly biased. When the threshold is reached (about 5 A at the 5 V output; about 500 mA at the $\pm$14 V outputs), the comparators switch (NPN open collector outputs) and bring about a lower make-to-break ratio; the corresponding output becomes the constant voltage source.

If the load increases (to a short circuit), the output voltages decrease. At 10 V at the 14 V output, the control IC switches off and the power source goes into the above-described cyclic "start test" mode.

The fourth comparator (IC 2) forms, with the thyristor TH 1, a "crowbar" circuit and protects the +5 V output from overvoltage (from the outside). The response threshold is about 5.5 V.

IC 1 produces the power-up and the power-down reset (system reset). Q1 and Q2 provide for the delayed switching on audio relay (located in AF 20).

Technical Data PS 20

Design	Single-ended flow transducer
Input	28 V/2 A
Output	1) 5 V/5 A 2) +14 V/500 mA (no-load voltage about 12.6 V) 3) -14 V/500 mA (no load voltage about 12.6 V) auxiliary voltages 1) -5 V/10 mA, -10 V/10 mA 2) -35 V/2 mA, -10 V/5 mA,
Operating frequency	about 100 kHz

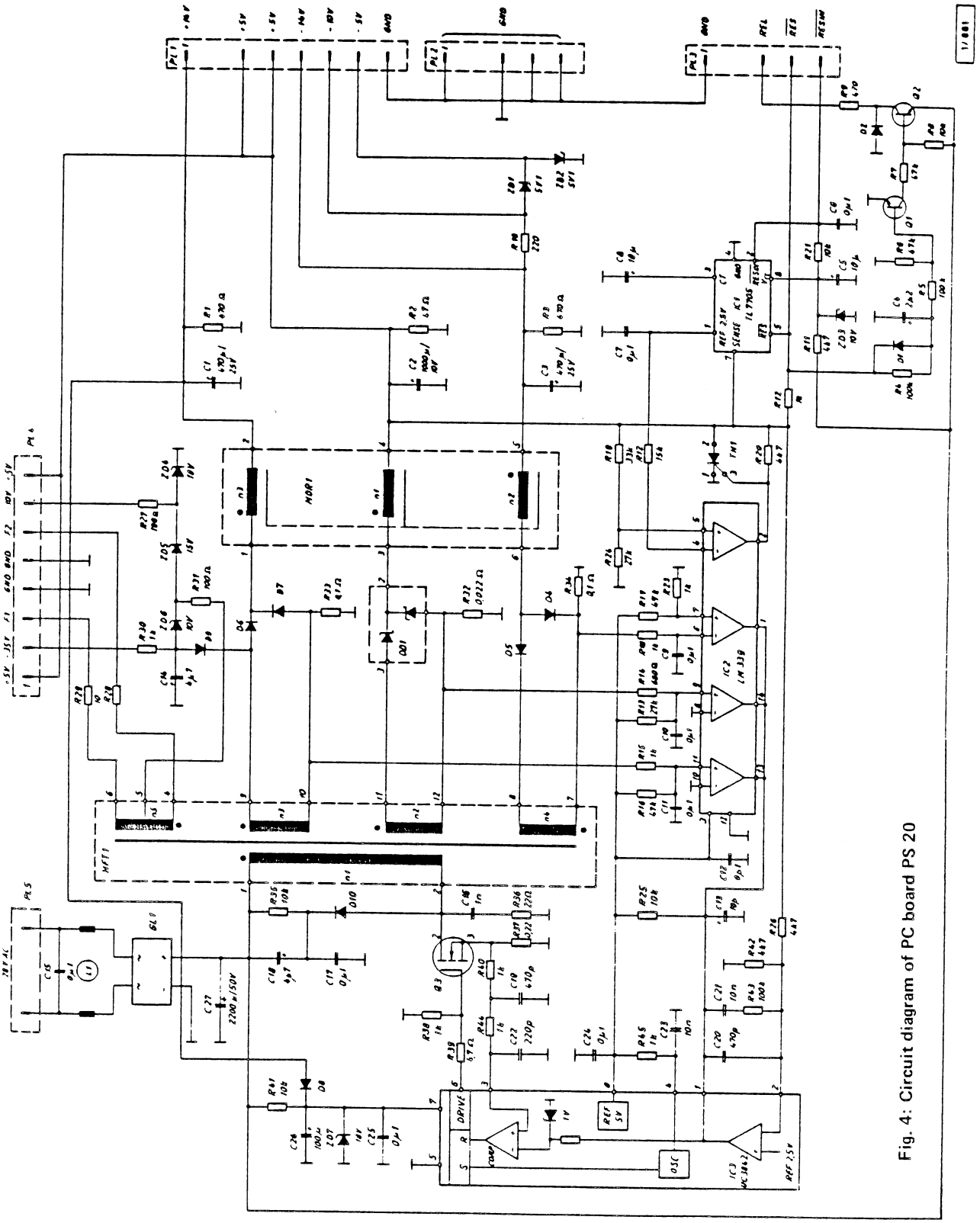


Fig. 4: Circuit diagram of PC board PS 20

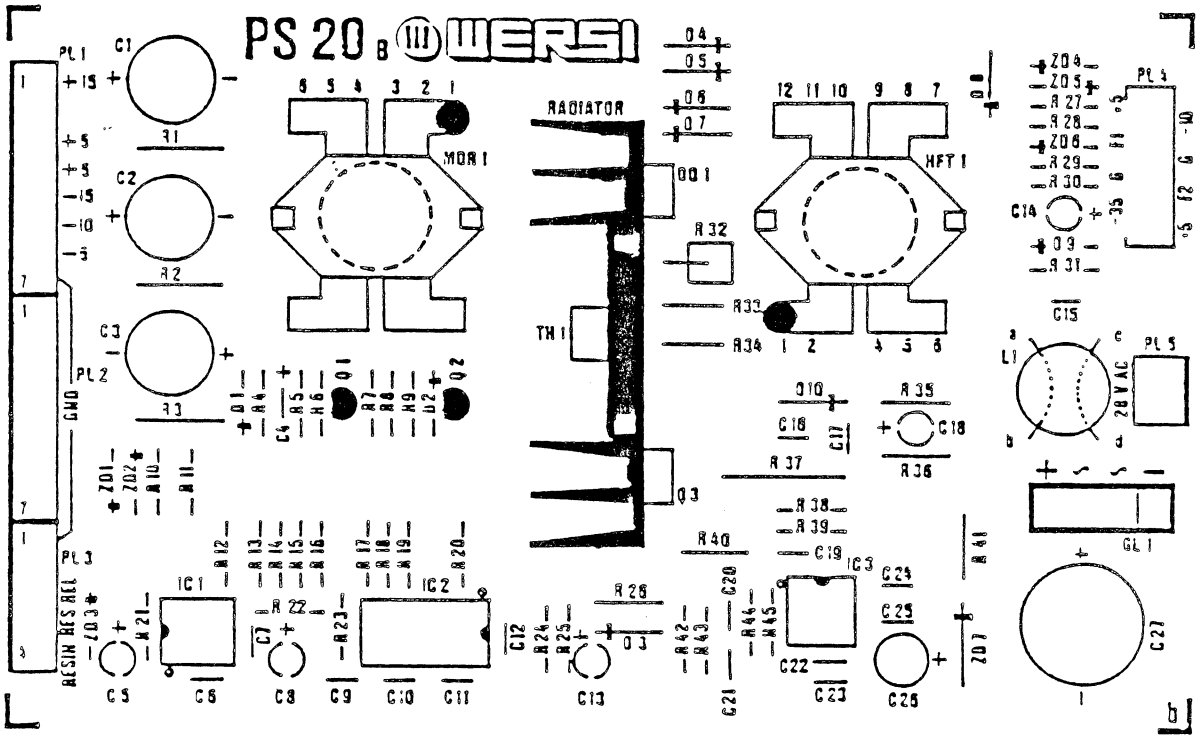


Fig. 5: Component layout of PS 20

B. Technical Description of PC Boards KD 10 and KD 4.

PC board KD 10 contains, together with PC board KD 4, the keyboard interrogation of the manual. A single chip microprocessor (IC 4), of a type similar to that in the slave, is responsible for all interrogation and outputting.

The dynamic measurement is based on the principle of time measurement. For this purpose, each key is connected to a switch. The time from the opening of the normally closed contact to the closing of the working contact is measured. 8 switches are combined in 1 matrix address. For 5 octaves (61 keys), 8 matrix addresses are needed. These matrix addresses are grounded one after the other, and the state at the 16 contacts is polled. The rate at which this polling occurs can be adjusted via the coding switch, which is polled only after resetting, however. If this time is very short, the key must be depressed very quickly for the loudest value to be reached. The data is transmitted to a 2 byte parallel port (IC 2, 3). The first port contains the pitch and whether the sound is to be switched on or off; the second contains the dynamic value. When the dynamic value is recorded, a flip-flop is set which prepares the keyboard interrupt, which is then released by the "enable-keyboard-interrupt" signal (ENKBQ). When the master CPU reads the second port, the flip-flop is reset. A new data transfer can begin.

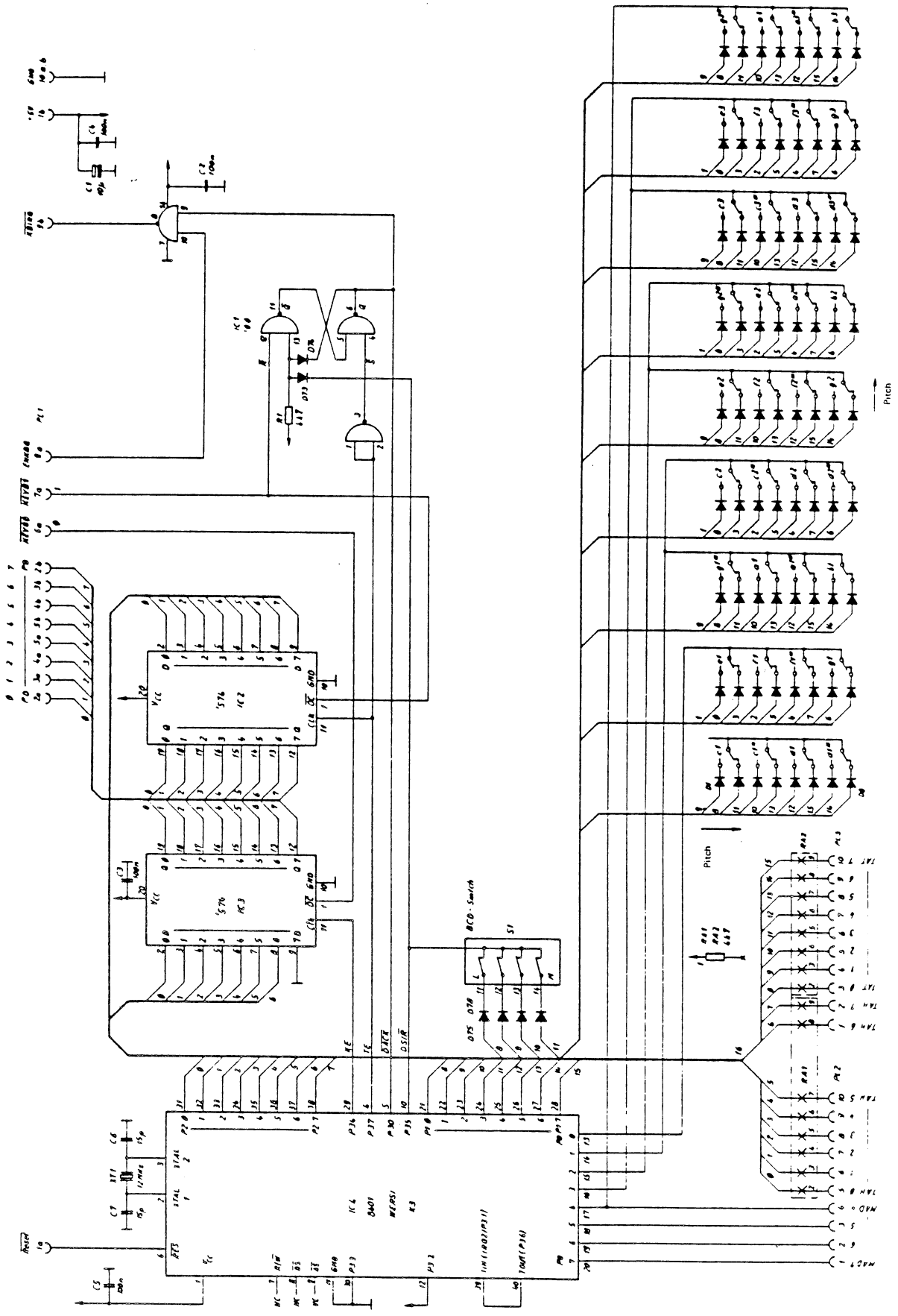


Fig. 6: Circuit diagram of PC board KD 10

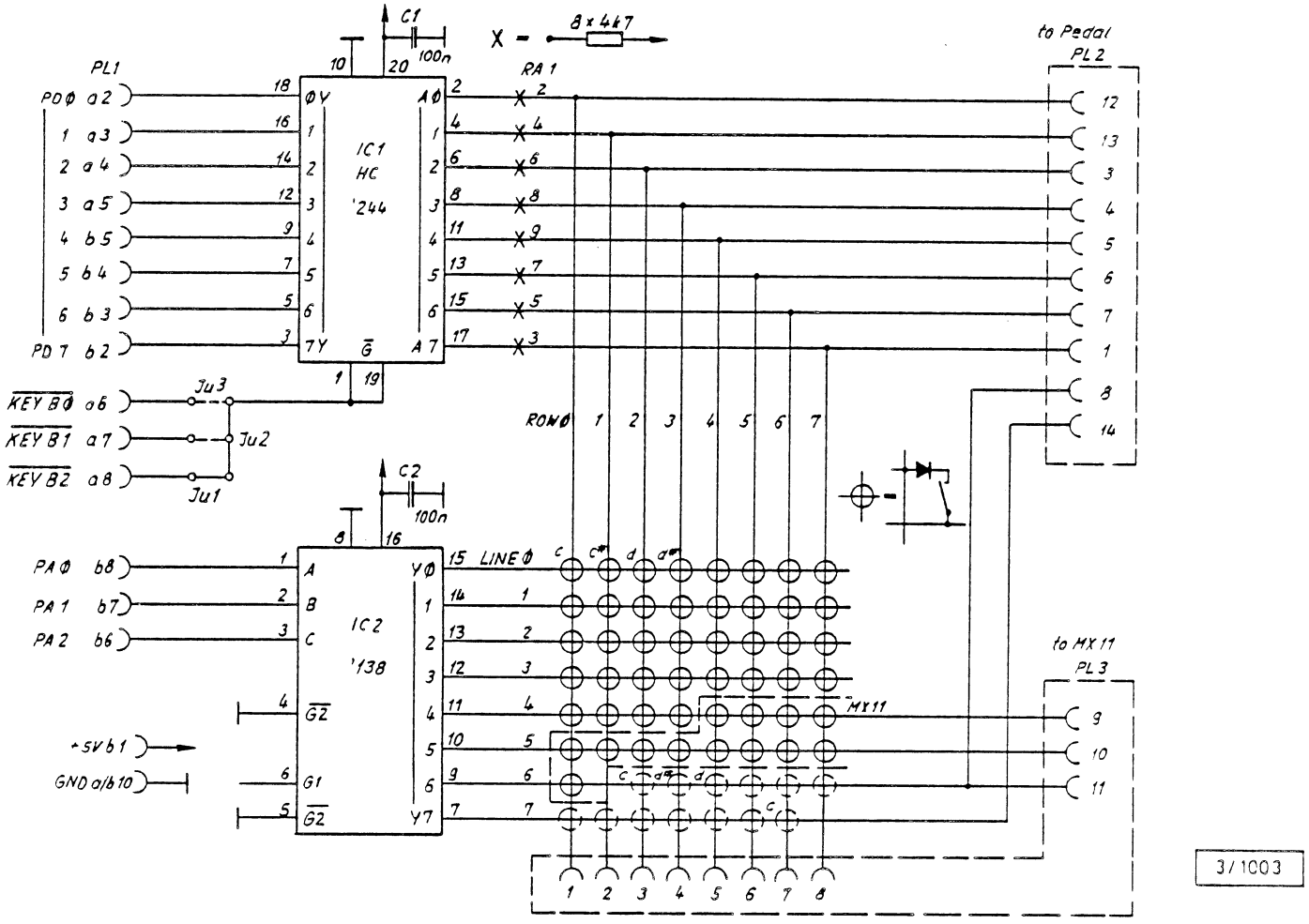


Fig. 6a: Circuit diagram of PC board MX 10

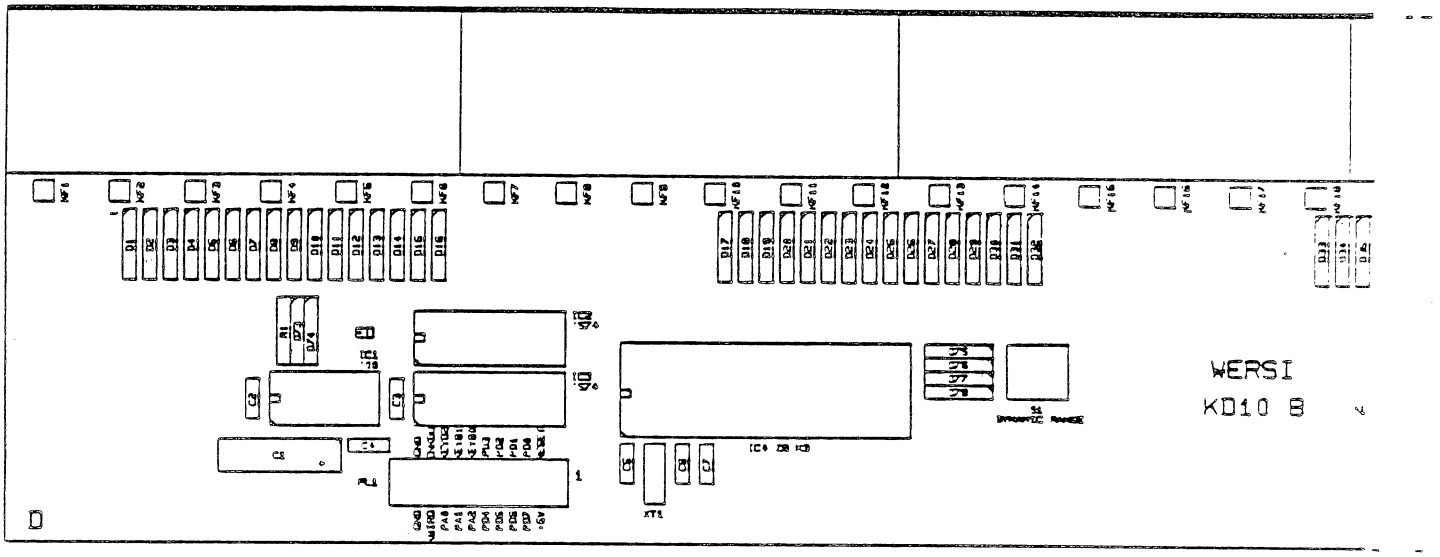


Fig. 7: Component layout of KD 10

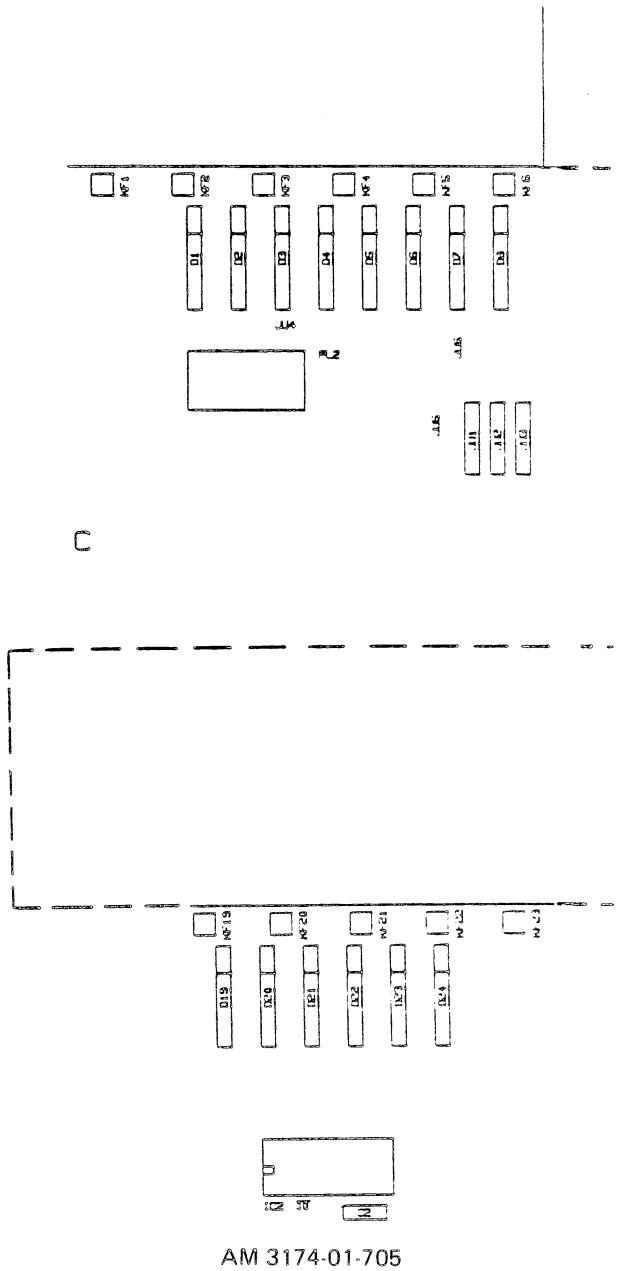
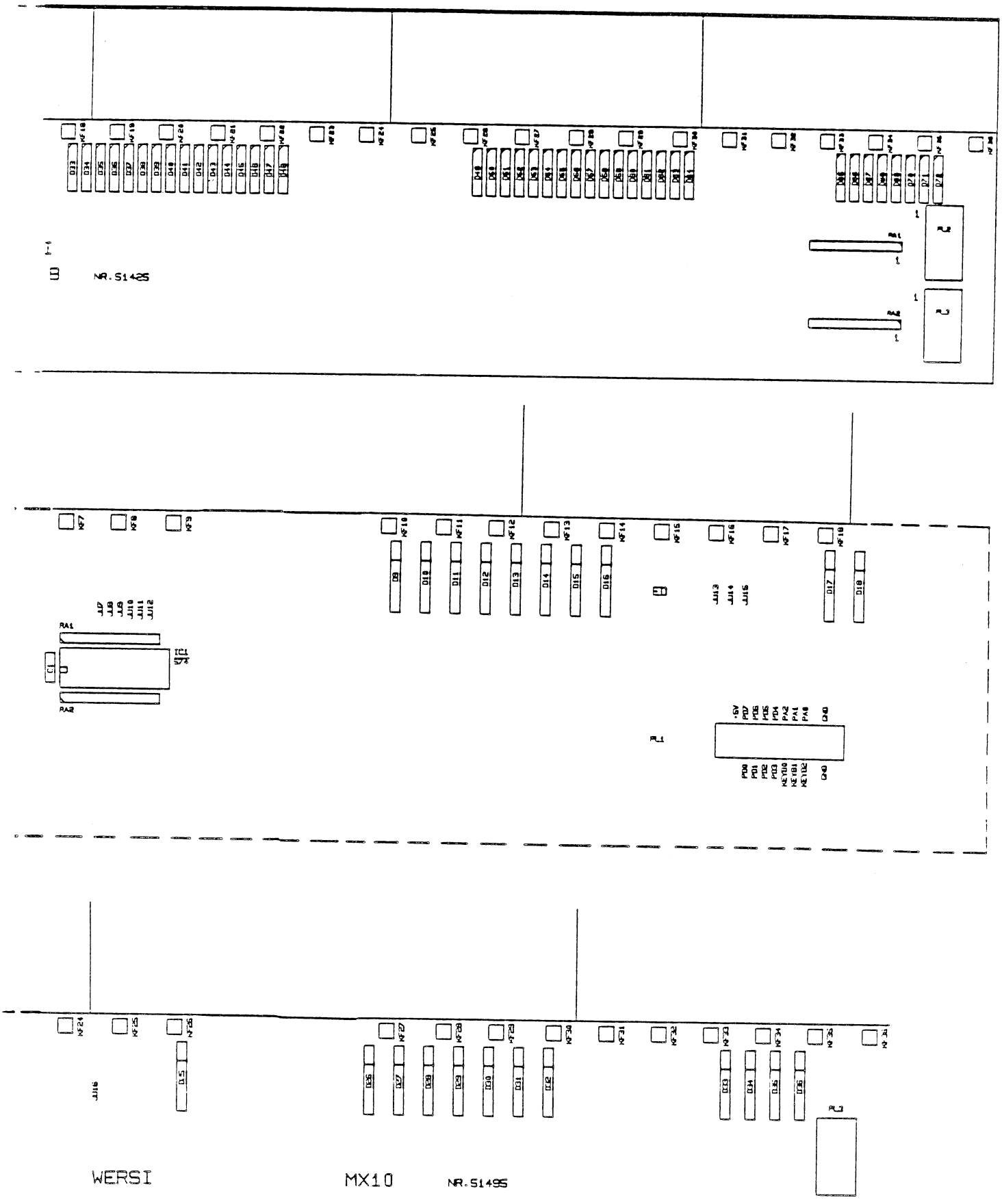


Fig. 7a: Component layout of MX 10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WERSI
MX10
NR.S1495

C. Technical Description of Control Electronics (in the EX 10, PC board ME 2 performs these functions)

1. The Identification and Output of the LED Switches (CBM 29, 30, 31, 36)

The outputting of all LEDs occurs in 6 groups of 16 elements each. Each group serially receives the information for each element, but all groups are operated in parallel, so after 16 clock cycles, all 96 switch LEDs have received their logic state. The groups are each made up of two 8-bit serial-in/parallel-out shift registers (CBM 29:IC 2, 3, 4/CBM 30:IC 7, 12; CBM 31:IC 1, 3, 4, 5, 6/CBM 36:IC 1, 2). PA Ø. . .PA 5 are the data signals of the 6 groups; Panclk is the serial shift clock, and with Panres, all units can be set to Ø.

The switch recognition is via comparators (CBM 29:IC 1/CBM 30:IC 8/CBM 31:IC 2/CBM 36: IC 3). By way of example, let us take a look at Group 1 (CBM 31); all other groups are identical in their function. If no switch is depressed, the voltage at pins 5 and 6 of IC 2 is determined only by the voltage dividers R 43 and R 50, since the switch outputs are open. A value of about 1.5 V appears. Due to the resistor chain R 47, 48, 49, the threshold of the upper comparator is set to 2.1 V and that of the lower comparator to 1.3 V; in other words, in this state all comparator outputs are pulled to +5 V by the pull-up resistors (R 44, 41). If a switch is closed, the input of the comparators (pins 5, 6) assumes a logic level (<.7 V or >2.4 V), and one of the comparators therefore switches through and triggers (possibly via D 1) a keydown signal (KD). As a result the master processor recognizes that some key has been depressed.

The master then deletes all shift registers with Panres and shifts only one logical 1 through all 16 stages. After each step, the sense line (sense Ø. . .5) is observed. If the logical 1 (2.4 V) reaches the depressed switch, the upper comparator switches the sense line to ground and the processor can then identify the switch number on the basis of the shift cycles. This procedure occurs in parallel for all groups, so after a maximum of 16 clock pulses, the switch and the group are located. With this procedure, however, only 1 single key depression can be recognized. The identification signals KD, sense Ø. . .5 are read by the CPU via the input port "panin" (CBM 30:IC 5). The serial shift data (PA Ø. . .5) are written into the "panout" latch (CBM 30:IC 9).

2. The Display (CBM 30)

The "panout" latch IC 9 also includes the data (DDat) and clock line (Dclk) for the display controller IC 11, which independently controls the 16-digit alphanumerical fluorescent display. The heating voltage for the display is provided by the power supply as a clocked signal. This voltage is also the cathode potential for the display signals.

3. Analog Data Acquisition (CBM 30)

Analog data (potentiometer data, touch, wheel, volume pedal) cannot be directly gathered by a microprocessor. They must first be transformed to digital data. This is done by an A/D converter (IC 6). However, the converter has only 1 analog input (pin 6). In order to gather the 24 analog values, the analog voltages are multiplexed by IC's 2, 3 and 4 before being applied to the input of the A/D converter.

4. The Keyboard Electronics (CBM 30)

The master decoding provides 3 select lines (KB Ø. . .2) for keyboard identification. Two select lines are required by the dynamic keyboard electronics on the KD 10 (key number, dynamic value). The lower keyboard is polled via KEYB 2.

D. Technical Description of PC Boards MX 10/11

The lower keyboard does not sense dynamics, but only whether keys have been turned on and off.

The main CPU selects a line Ø. . .7 at IC 2 via peripheral address PA Ø. . .PA 2 and also polls Row Ø. . .7 via IC 1. By being able to poll both lines and rows, the CPU can detect which key is depressed.

The 13 pedals can also be recognized at the same-time.

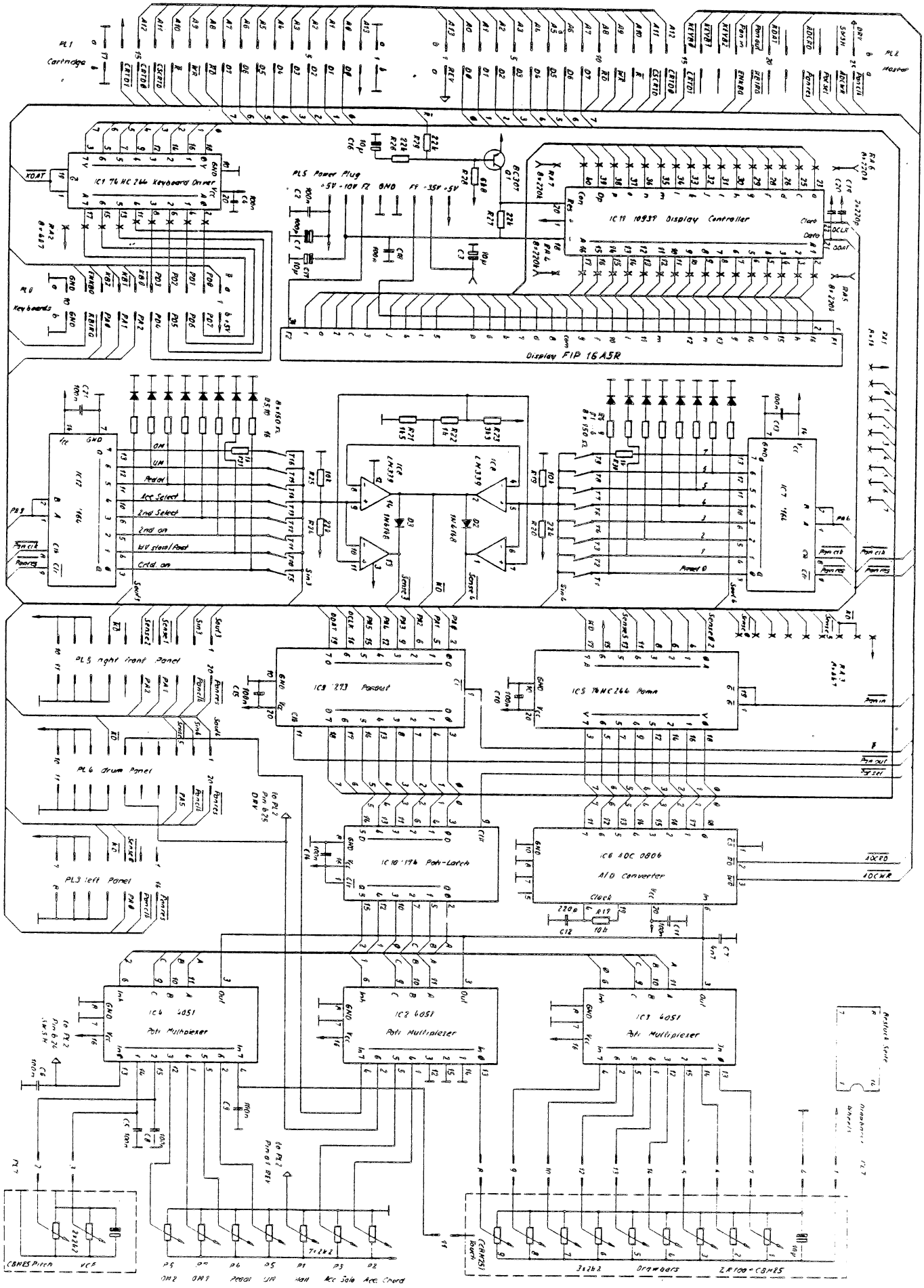


Fig. 8: Circuit diagram of PC board CBM 30

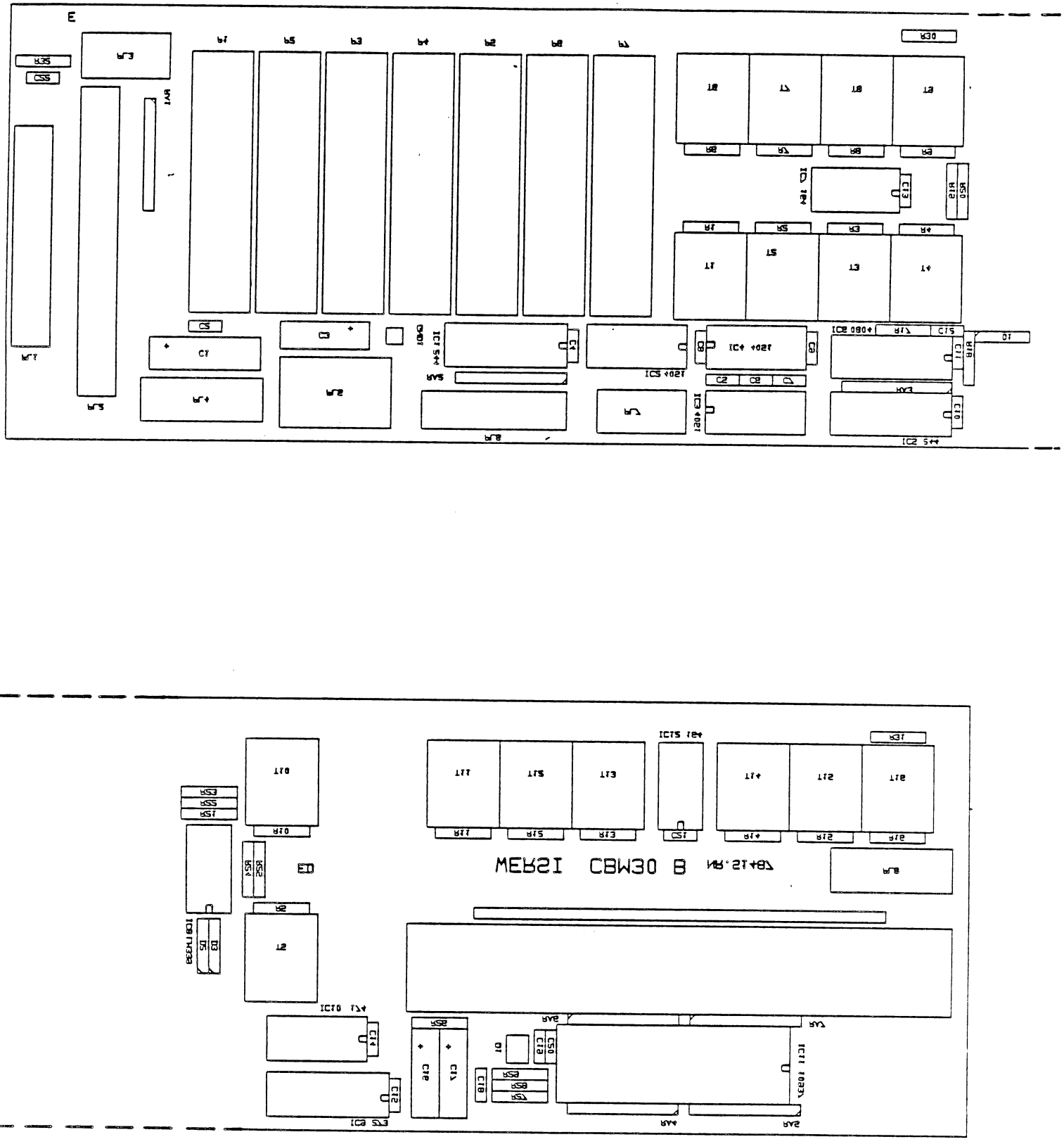


Fig. 9: Component layout of CBM 30, x-ray view from solder side.

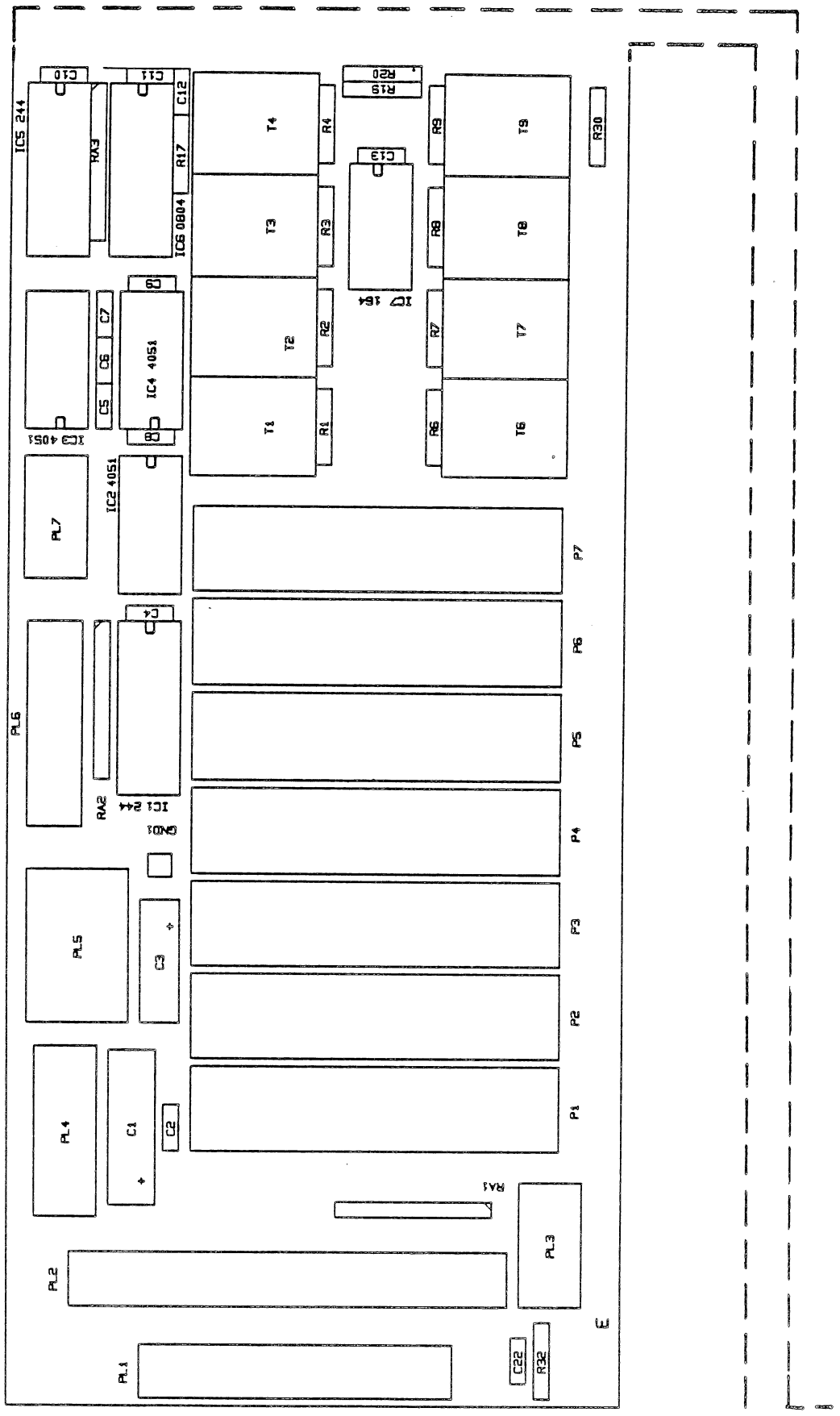
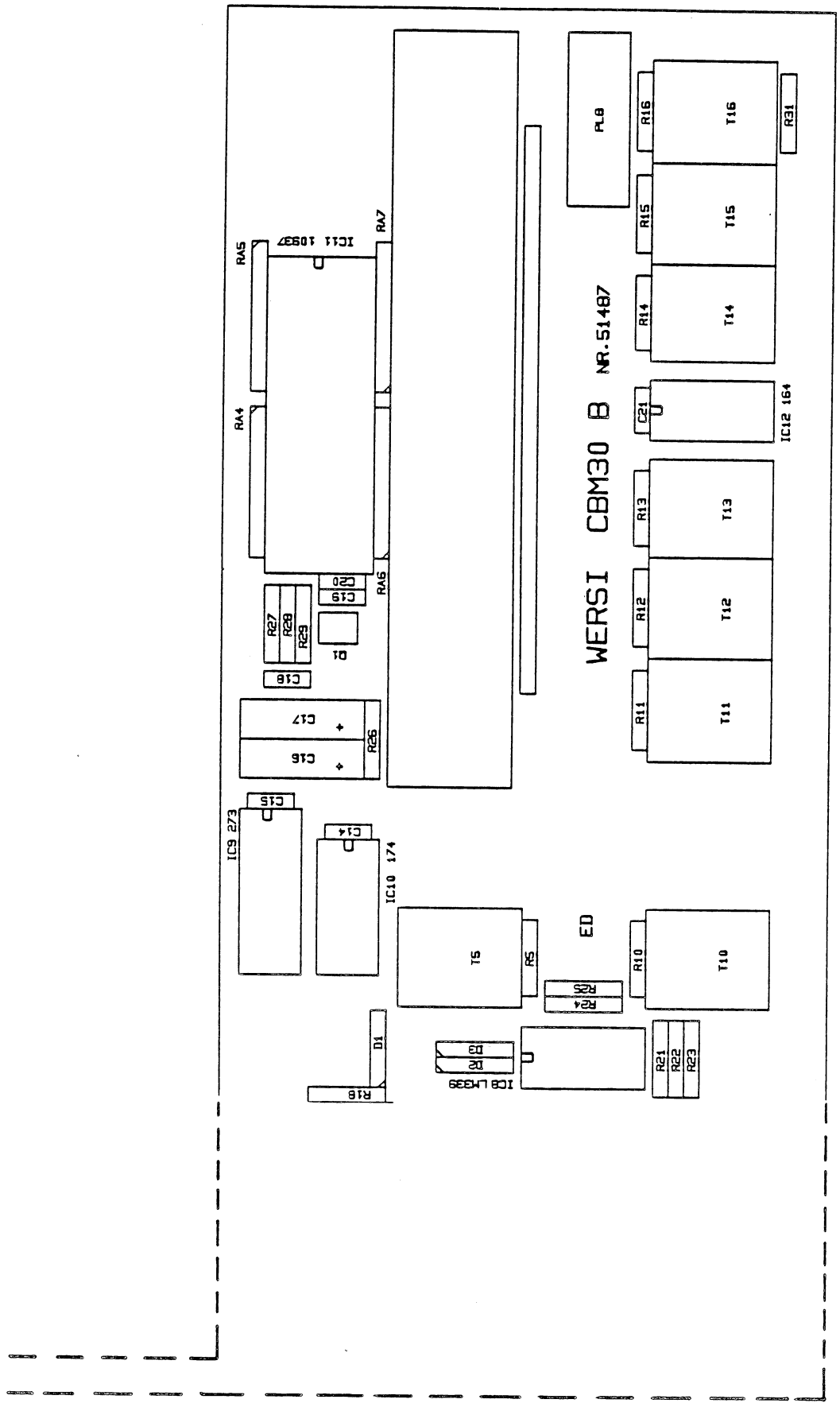


Fig. 10: Component layout of CBM 30


WERSI CBM30 B NR.51487
IC11 1093?
RA5
RA7
RA4
RA6
C20
C19
R27
R28
R29
D1
C18
C17
C16
R26
C15
IC9 273
C14
IC10 174
T5
R5
R24
R25
R10
T10
D1
R18
IC8 LM339
R21
R22
R23
ED
PL8
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IC12 164
R13
T13
R12
T12
R11
T11

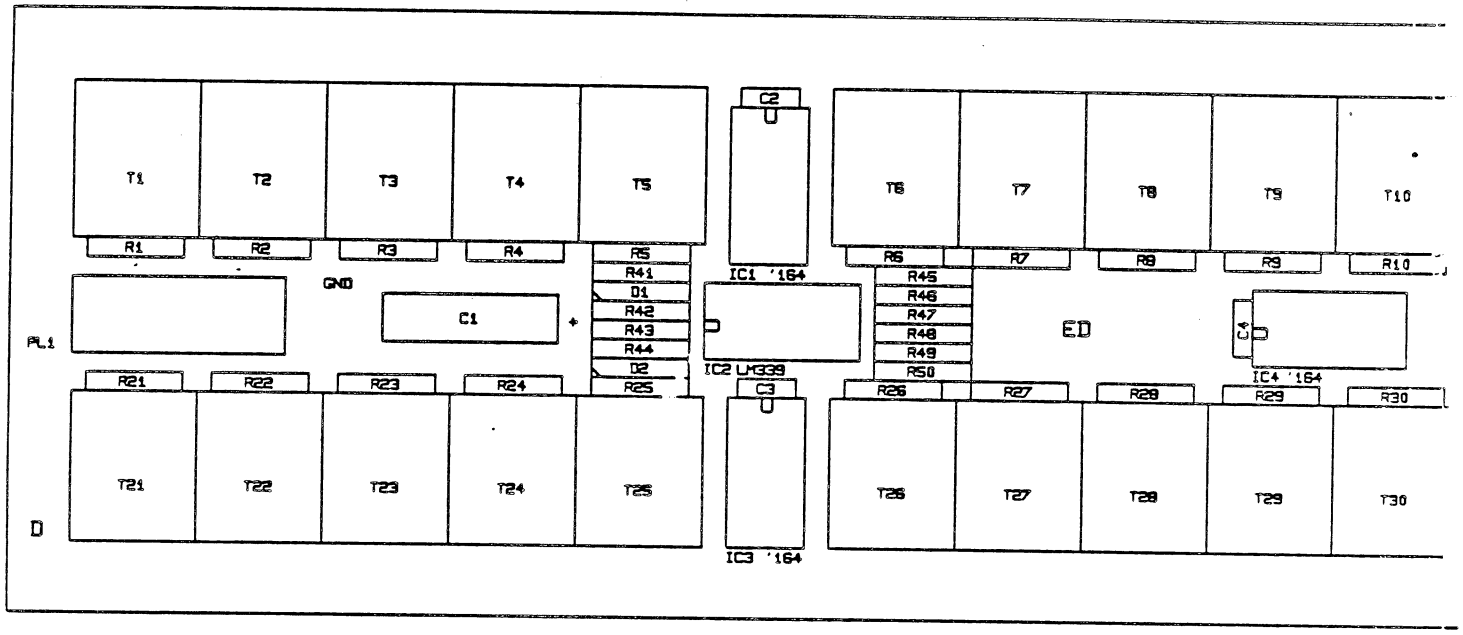


Fig. 11: Component layout of CBM 31

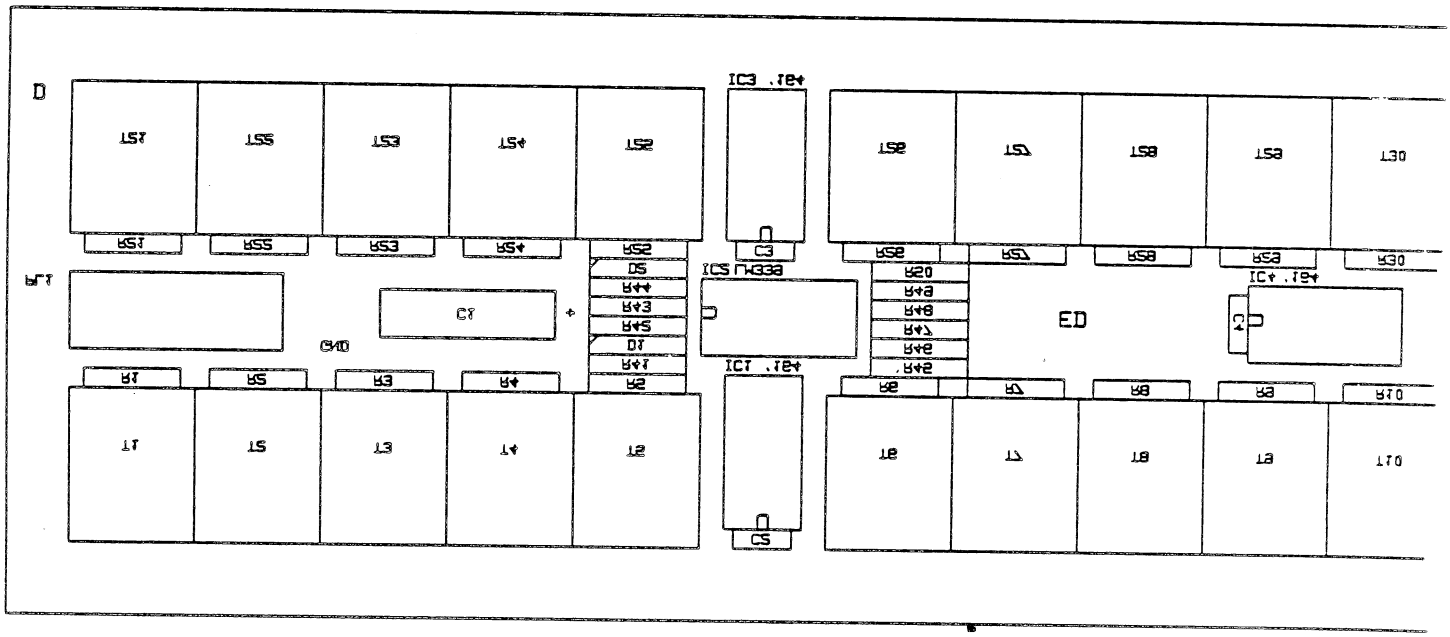
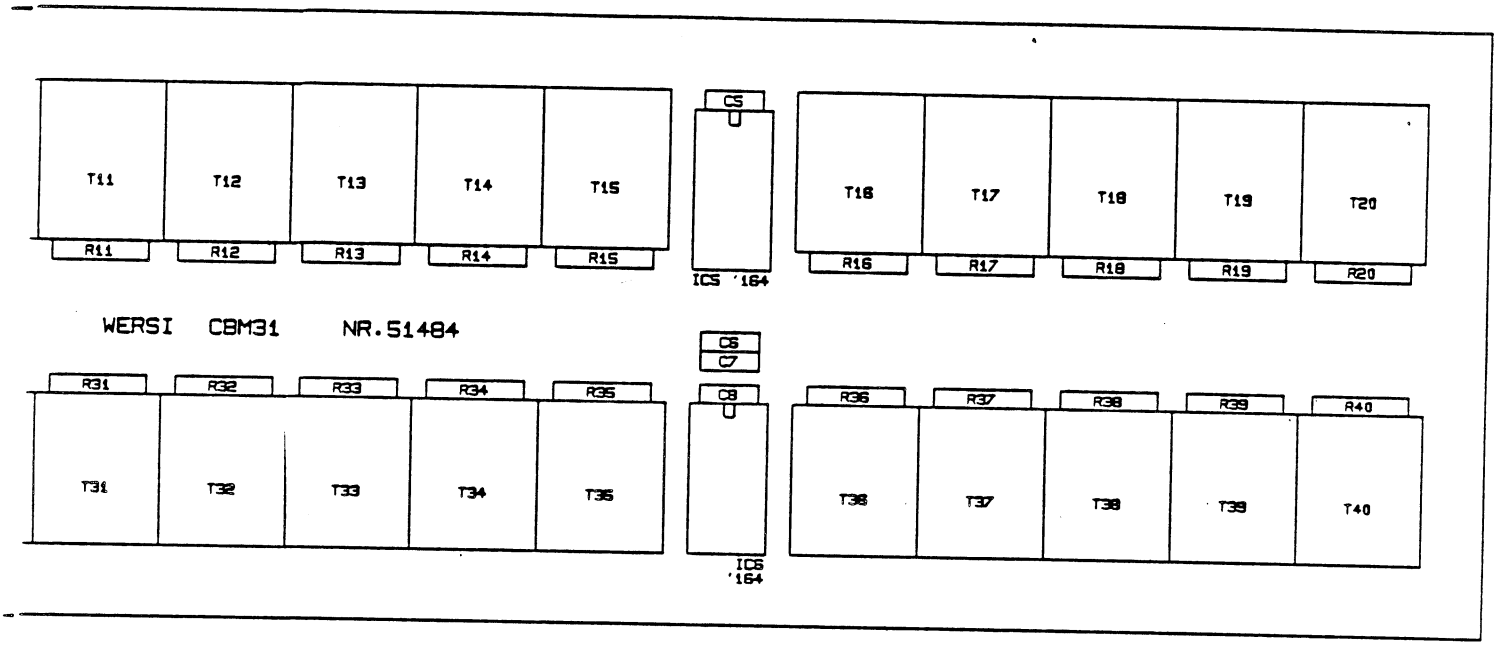
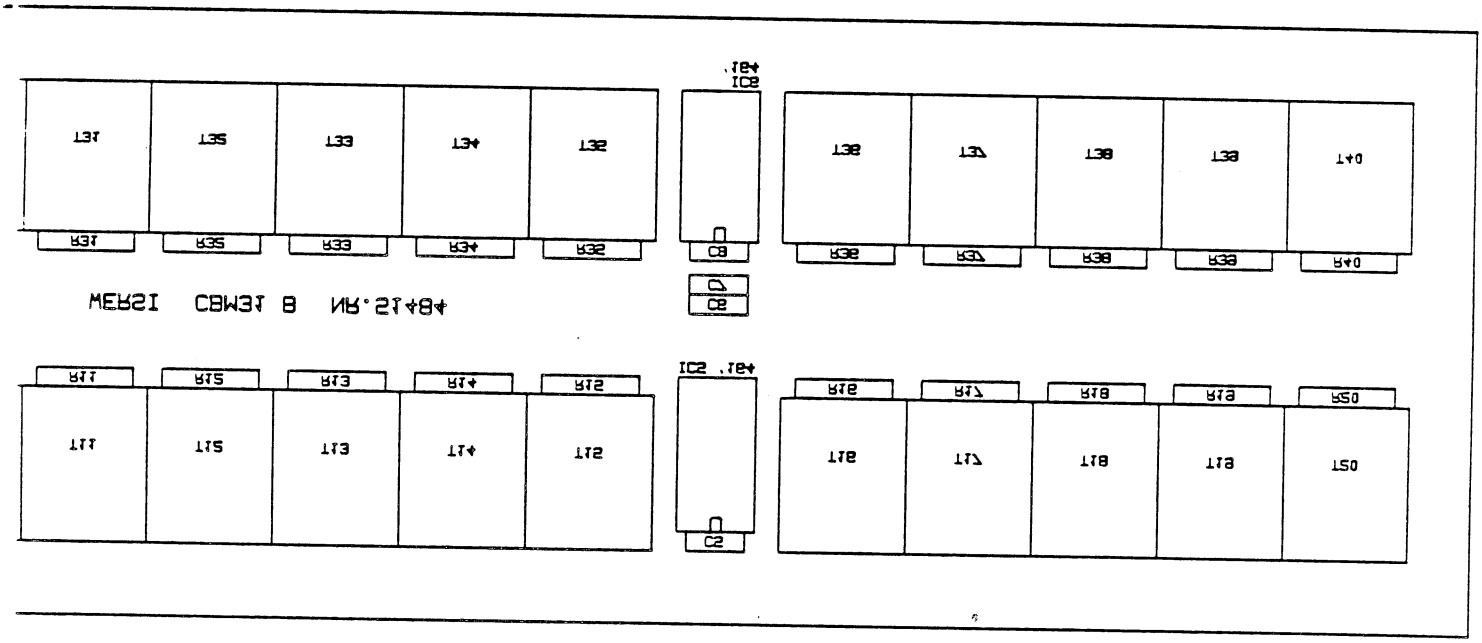


Fig. 12: Component layout of CBM 31, x-ray view from solder side.





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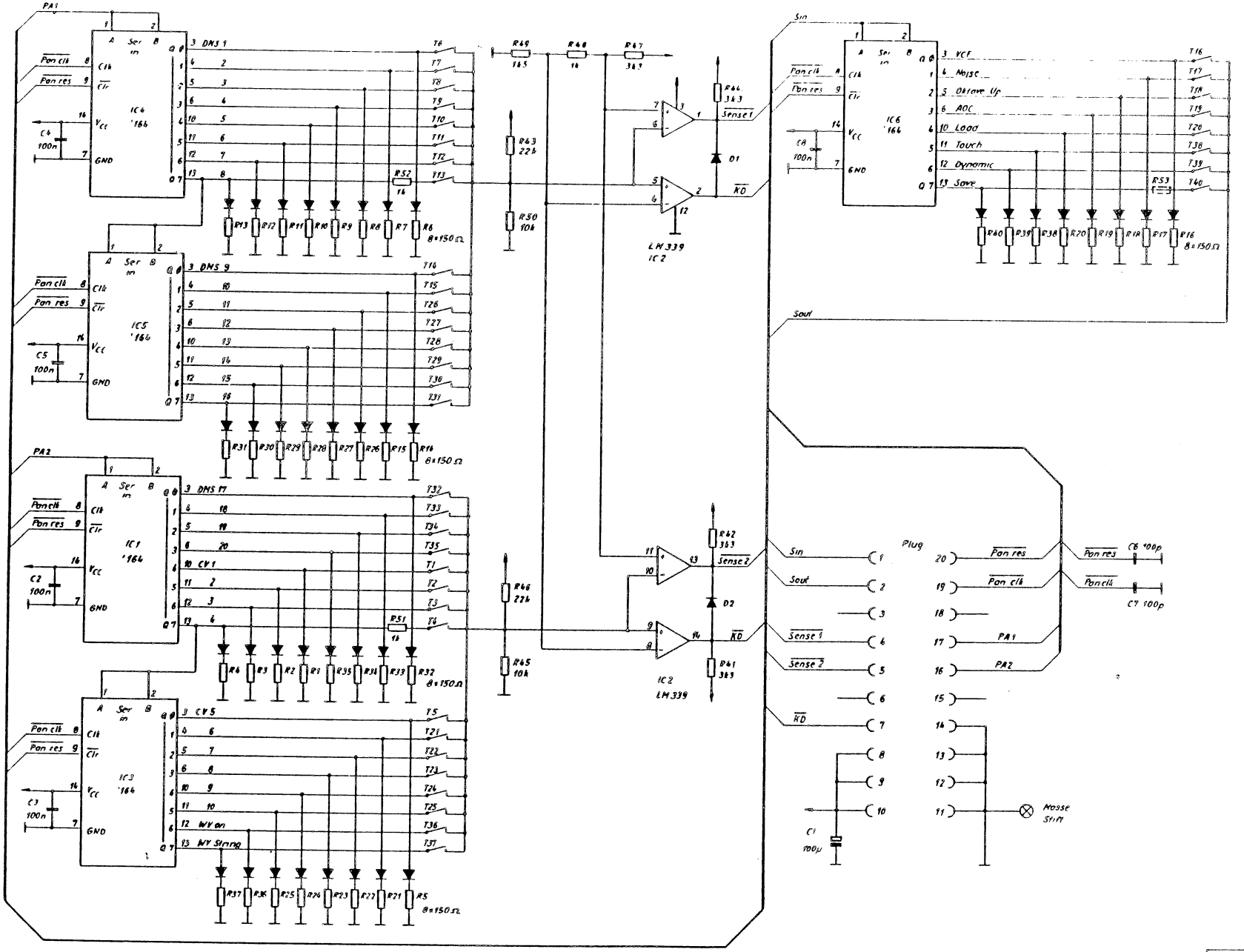


Fig. 13: Circuit diagram of PC board CBM 31

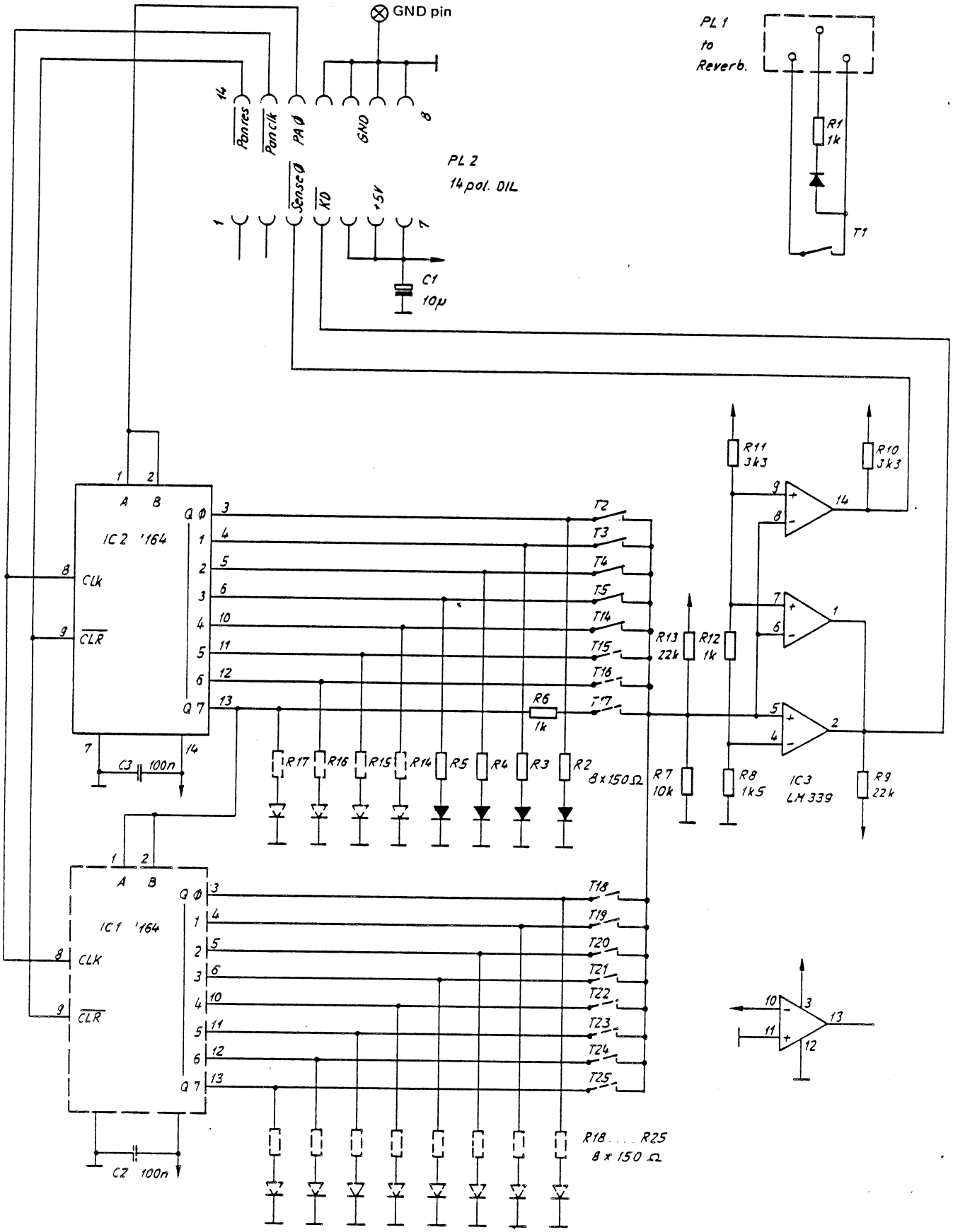


Fig. 13a: Circuit diagram of PC board CBM 36

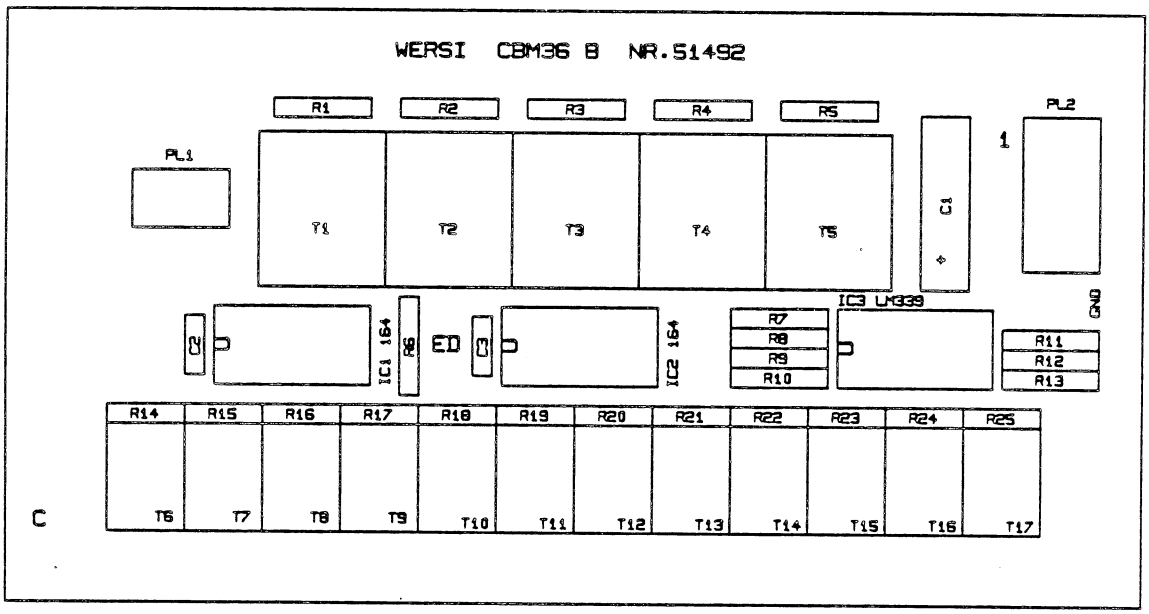


Fig. 13b: Component layout of CBM 36

E. Technical Description of PC Board CB 320 (EX 10 R) and CBM 32 (OMEGA)

On the connection PC board CB 320/CBM 32 there are several independent circuits for adapting external components to the keyboard. The components referred to in the description below applies to CB 320.

1) Headphone Amplifier:

Audio (AF) signals via PL 10, L 4, L 5, IC 1 (TL 082) with the transistors Q 1/Q 2 and Q 3/Q 4 switched as a push-pull stage, via the protective resistors R 2 and R 6 (100 Ohm, 2 W) to the stereo jack PL 1.

2) Audio Outputs, Stereo/L Jack PL 8 and Mono Jack PL 9 (Mono/R).

a) If 2 separate mono cables are plugged into PL 8 and PL 9, then the R and L channels are separate, with one channel in its respective jack.

b) If only 1 stereo cable is plugged into the jack Stereo/L: the 2 channels are available separately via a stereo line.

c) If only 1 mono cable is plugged into the jack Mono/R: the 2 channels are combined and available as a mono signal.

Switch (S 1) is also provided for switching the output level at the audio jacks (high-low). Voltage dividers R 35 to R 38 achieve this.

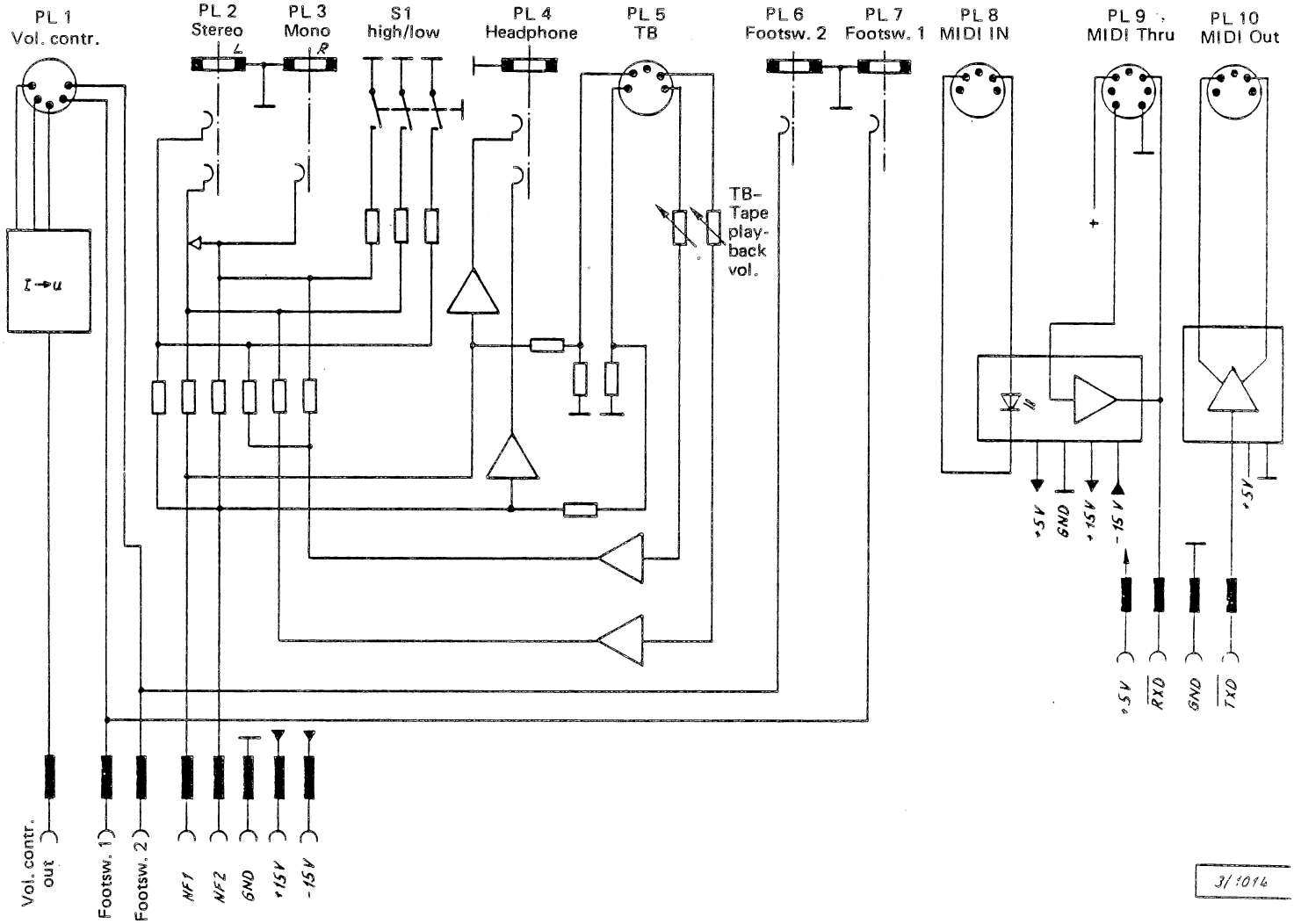


Fig. 14a: Block diagram of PC board CBM 32

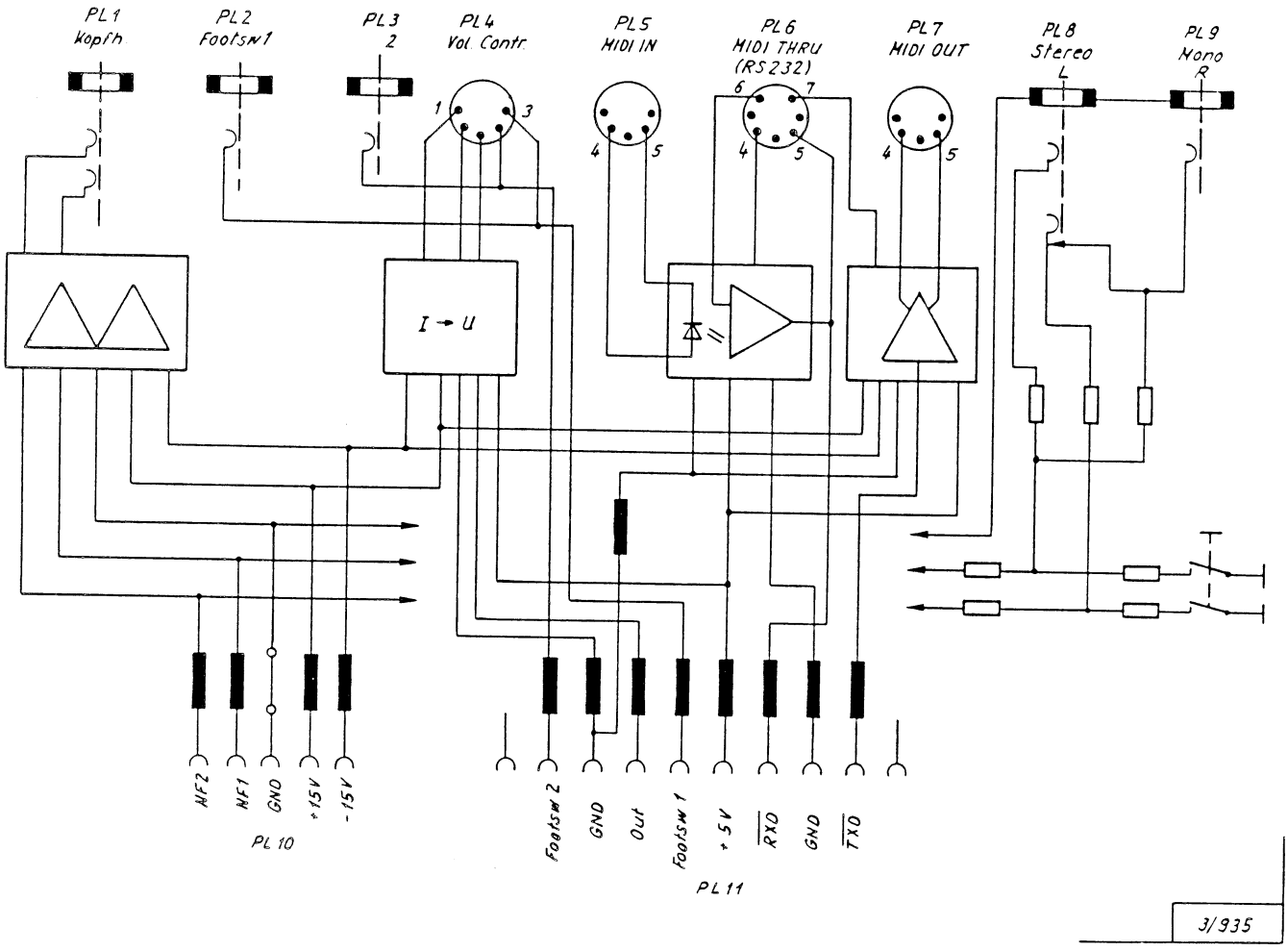


Fig. 14b: Block diagram of PC board CB 320

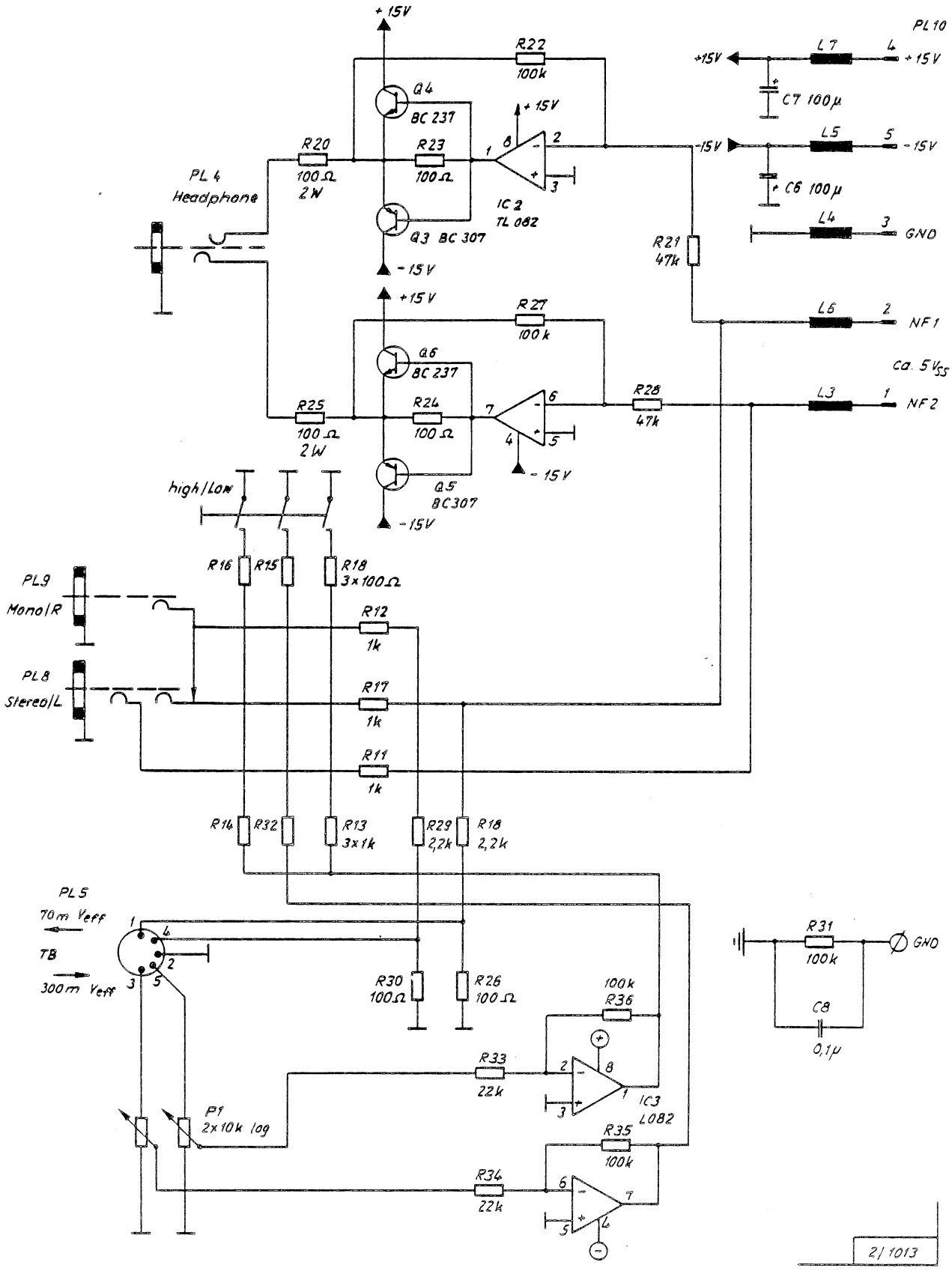


Fig. 15a: Partial circuit diagram of CBM 32 – Headphones

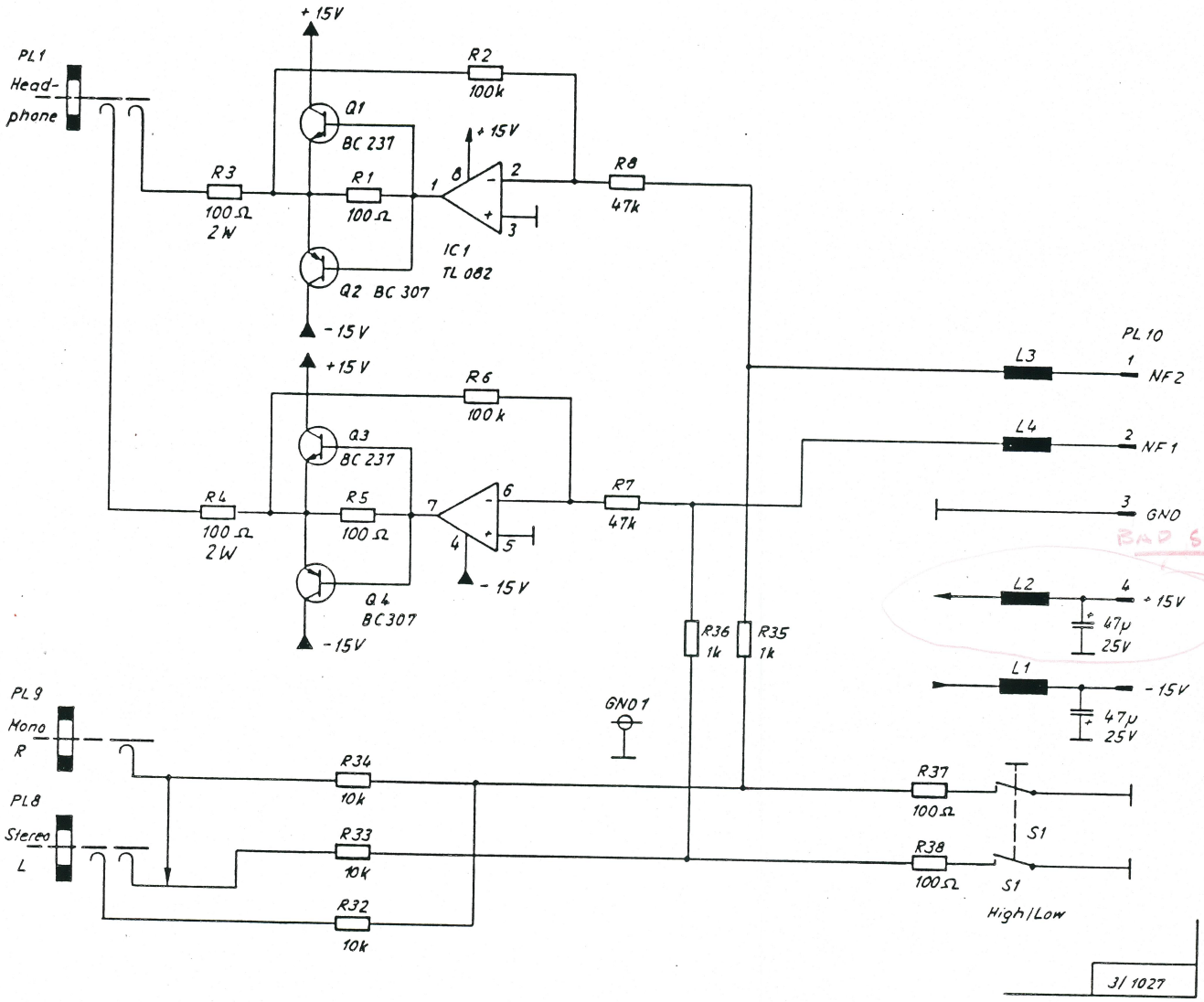


Fig. 15b: Partial circuit diagram of CB 320 – Headphones

3) Volume Pedal and Foot Switches:

The foot switches at the volume pedal and the separate foot switches (PL 2 and PL 3) are wired in parallel and switched to ground via L 7 and L 8 to PL 11, pin 2 (S2) and PL 11, pin 5 (S1).

The volume pedal (5-pin DIN jack, PL 4) operates in the region GND/–15 V. IC 2 (TL 081) and Q 6 convert the control voltage to the range 0 V/+5 V (0 V = low volume), via L 5 to PL 11, pin 4 (out).

Q 5, R 10 and R 11 determine whether a volume pedal has been plugged in. If no volume pedal connection is made, the control voltage goes to about +5 V (loud).

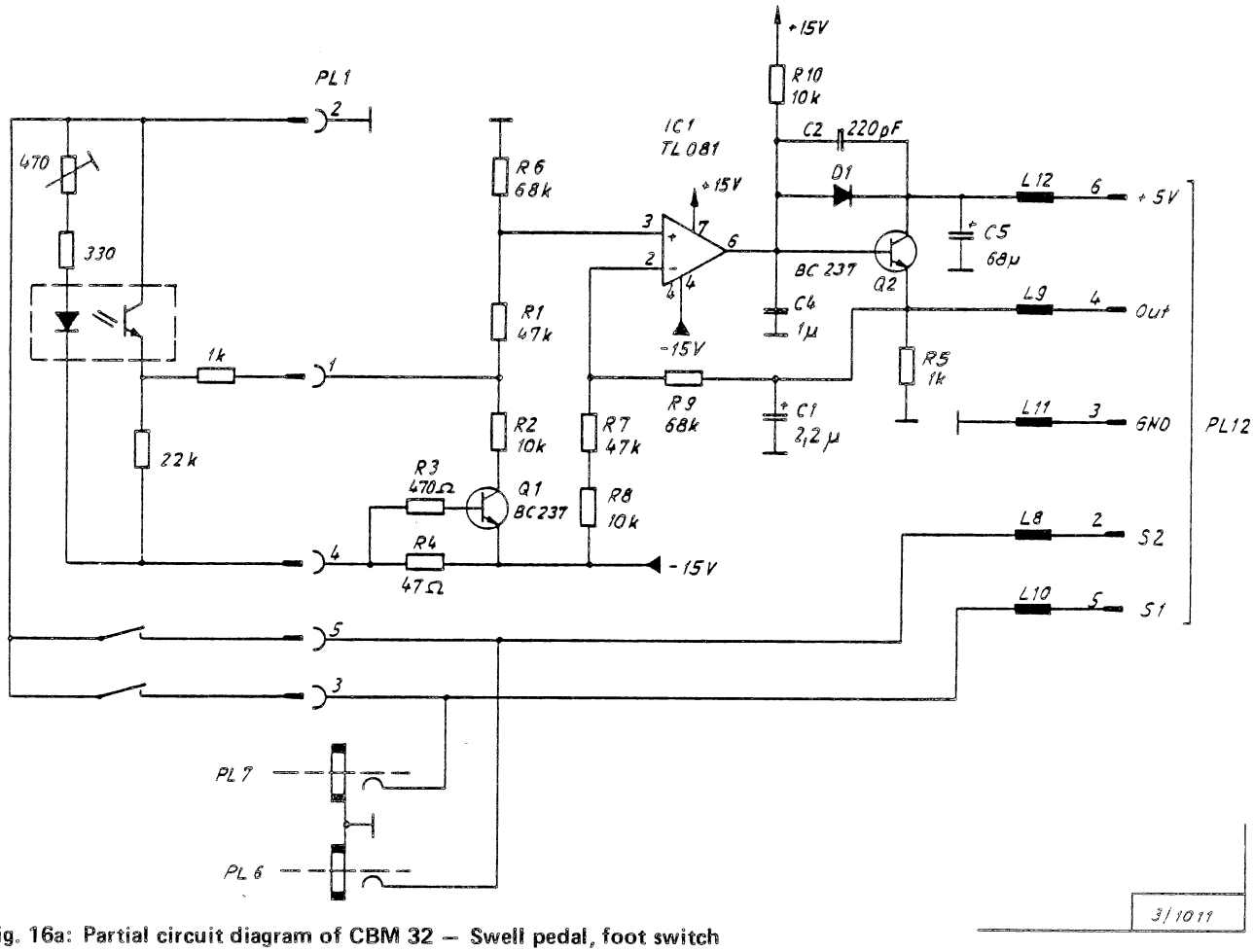


Fig. 16a: Partial circuit diagram of CBM 32 – Swell pedal, foot switch

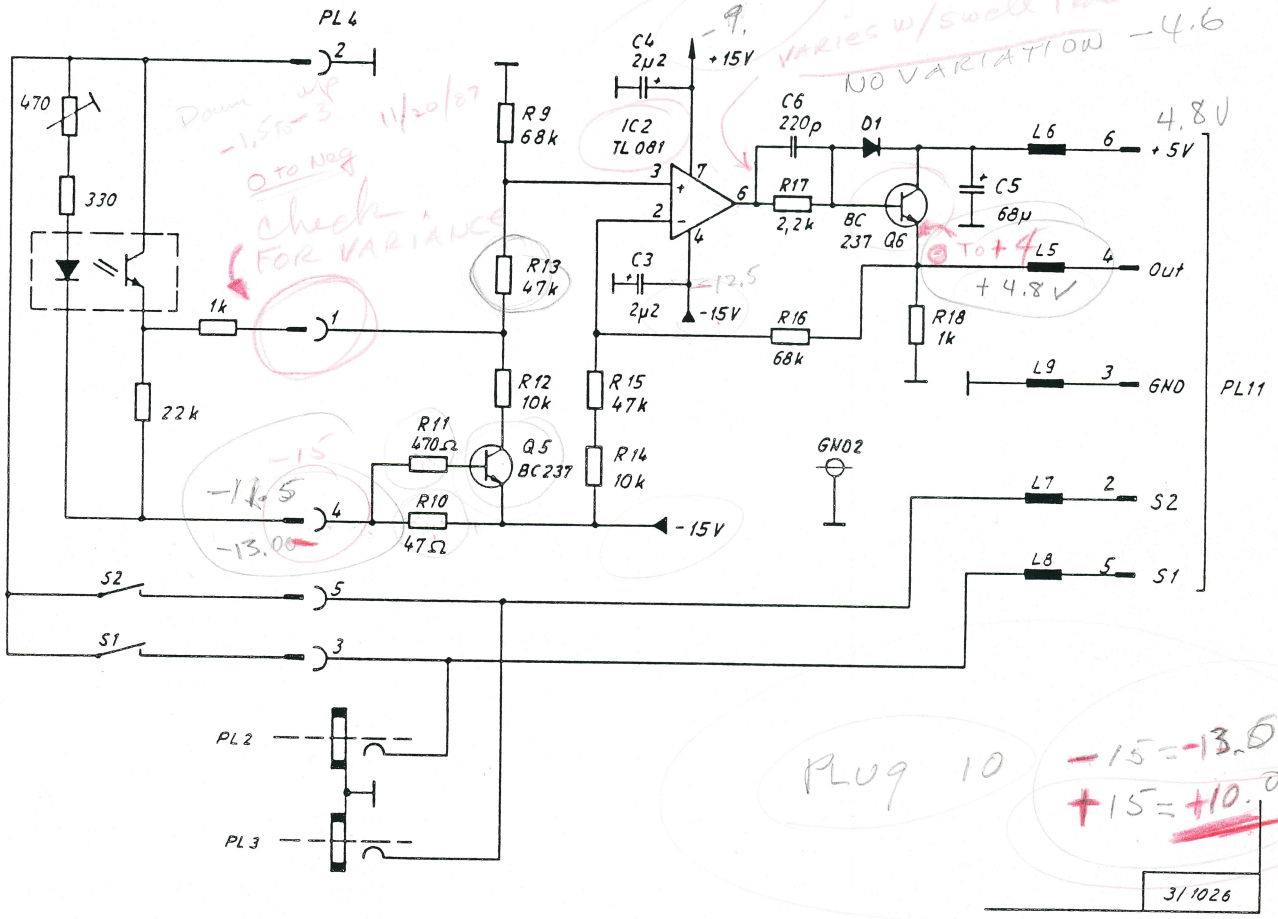


Fig. 16b: Partial circuit diagram of CB 320 – Swell pedal, foot switch

4) M.I.D.I. Interface

MIDI IN (PL 5) via protective circuit R 19, D 2 and IC 3 (optocoupler PC 910) or IC 4 (74 HCU 04) or PL 6 (MIDI THRU) and L 13 and PL 11, 7 (RDX).

MIDI OUT from PL 11, 9 (TDX), L 11, IC 4 and R 26, R 24 and PL 7 (MIDI OUT).

In addition, pin 7 TXD is connected to PL 6 (MIDI THRU), or RXD can be received via pin 6 (voltages correspond to RS 232).

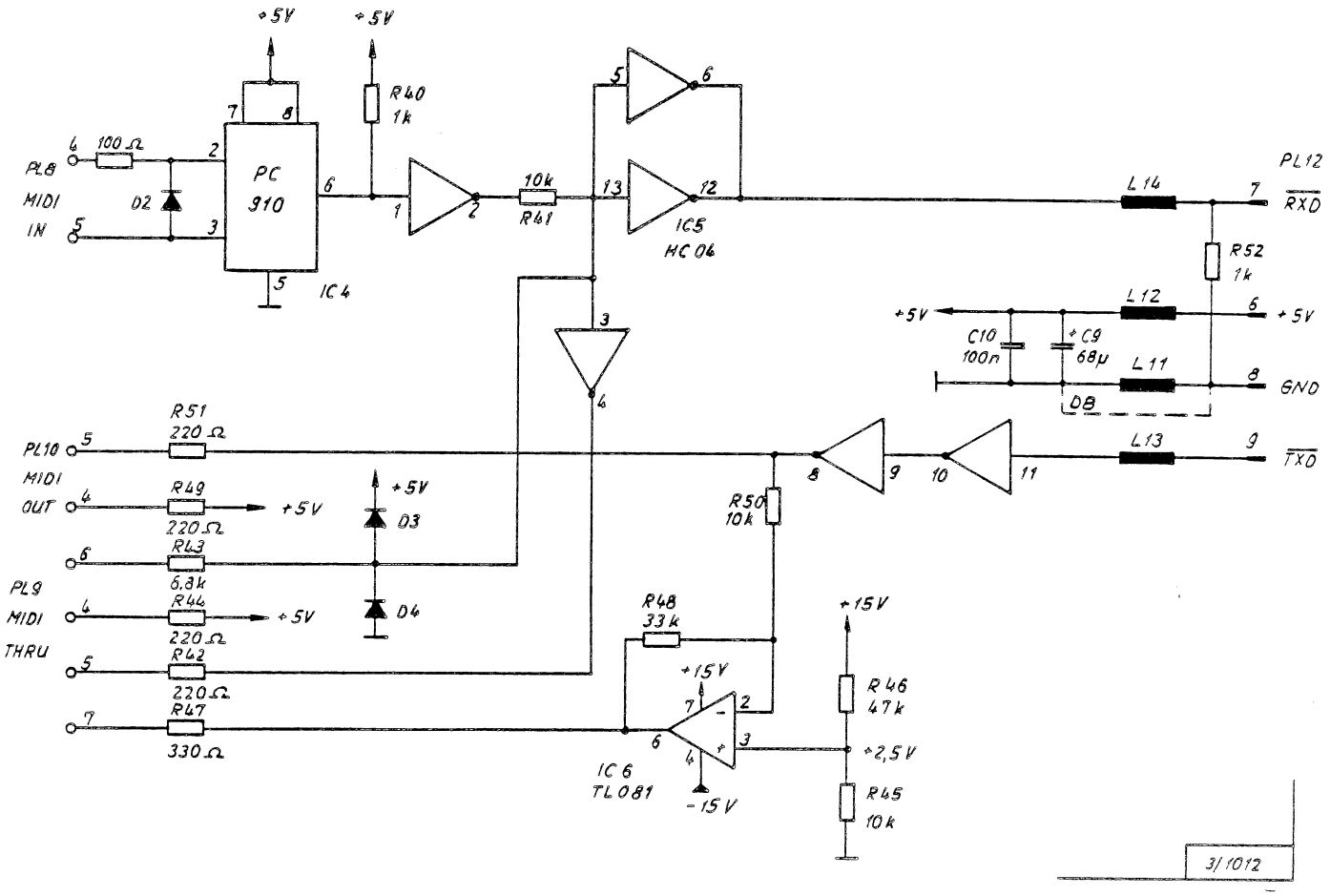


Fig. 17a: Partial circuit diagram of CBM 32 – MIDI

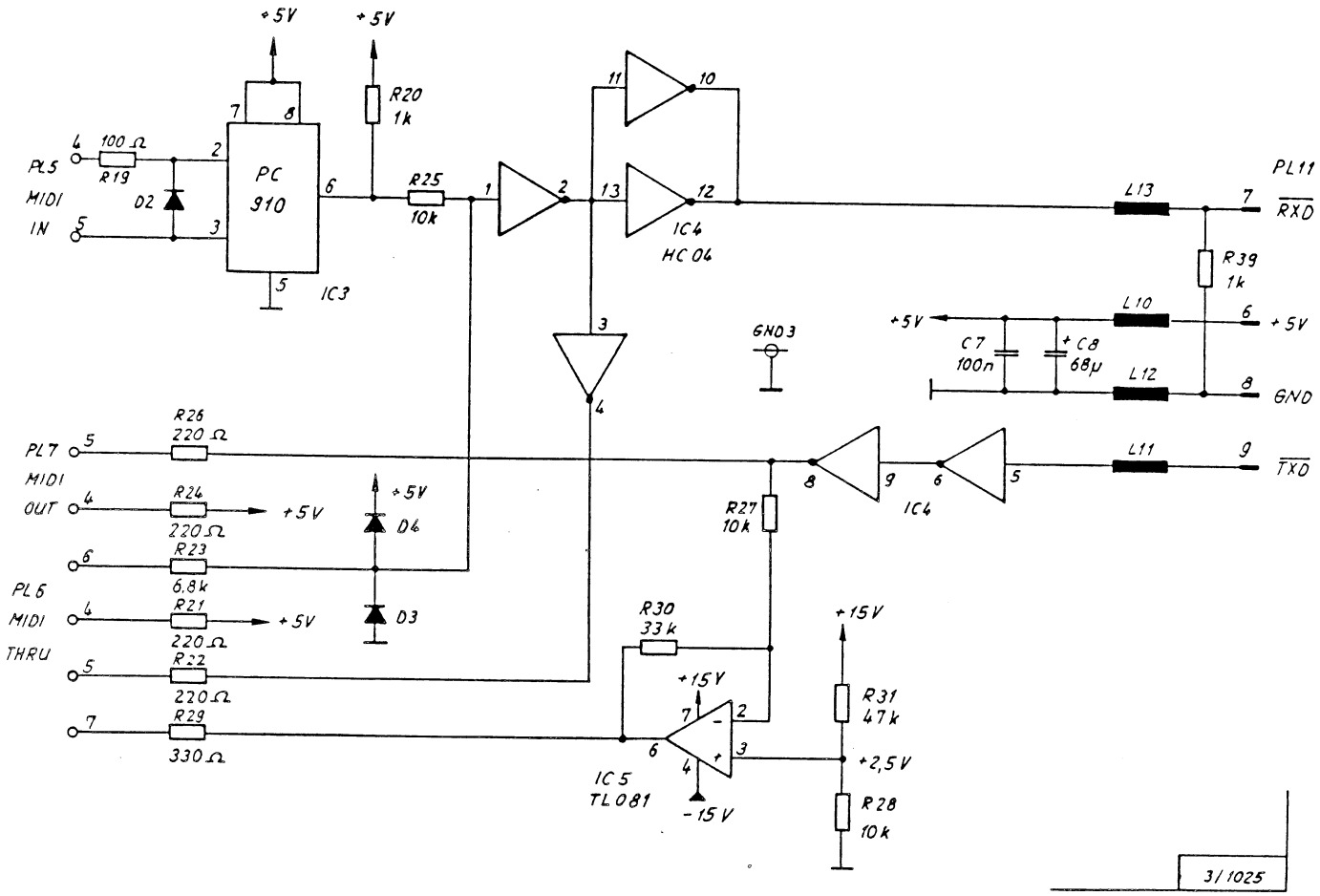


Fig. 17b: Partial circuit diagram of CB 320 – MIDI

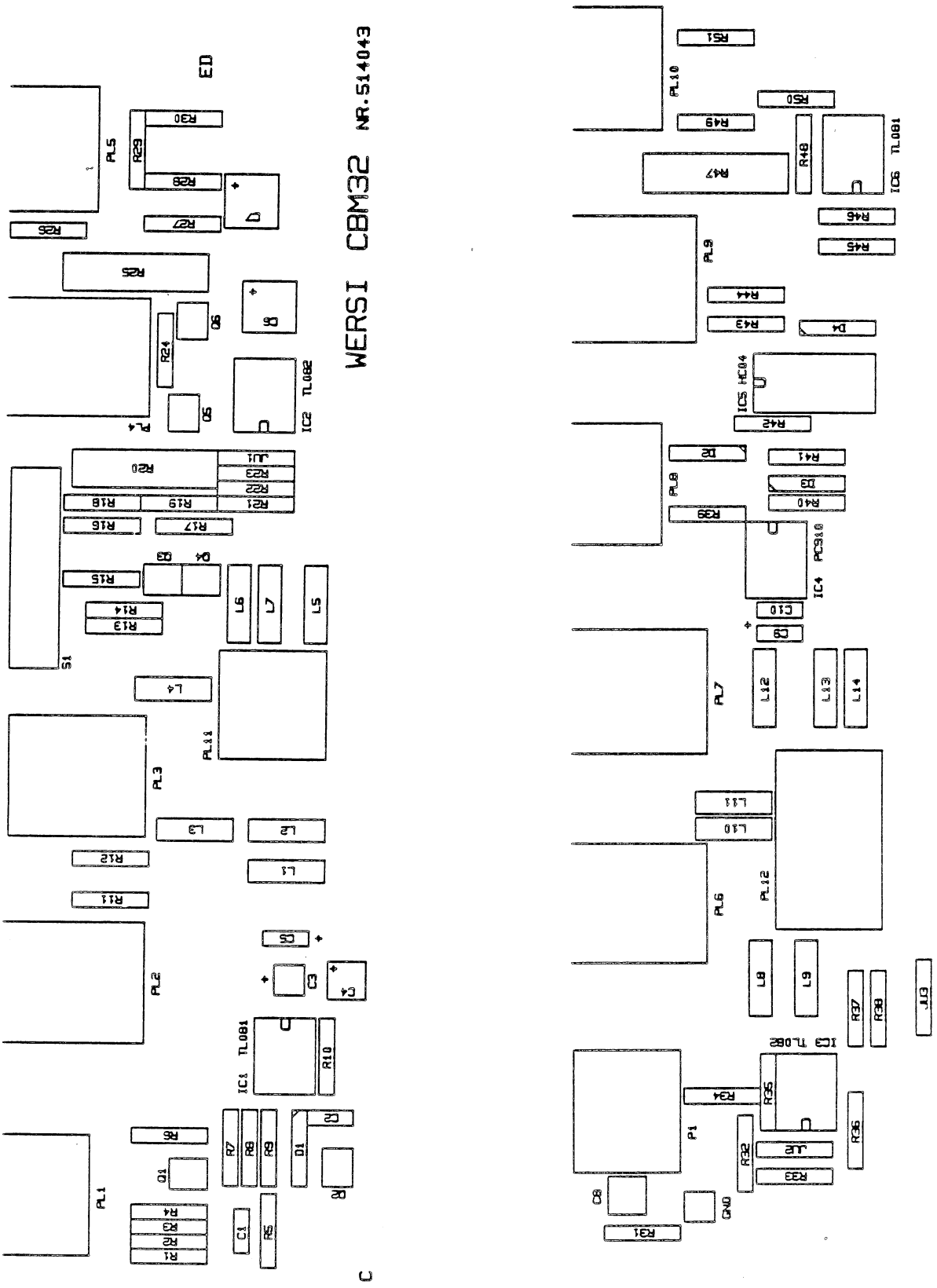


Fig. 18a: Component layout of CBM 32

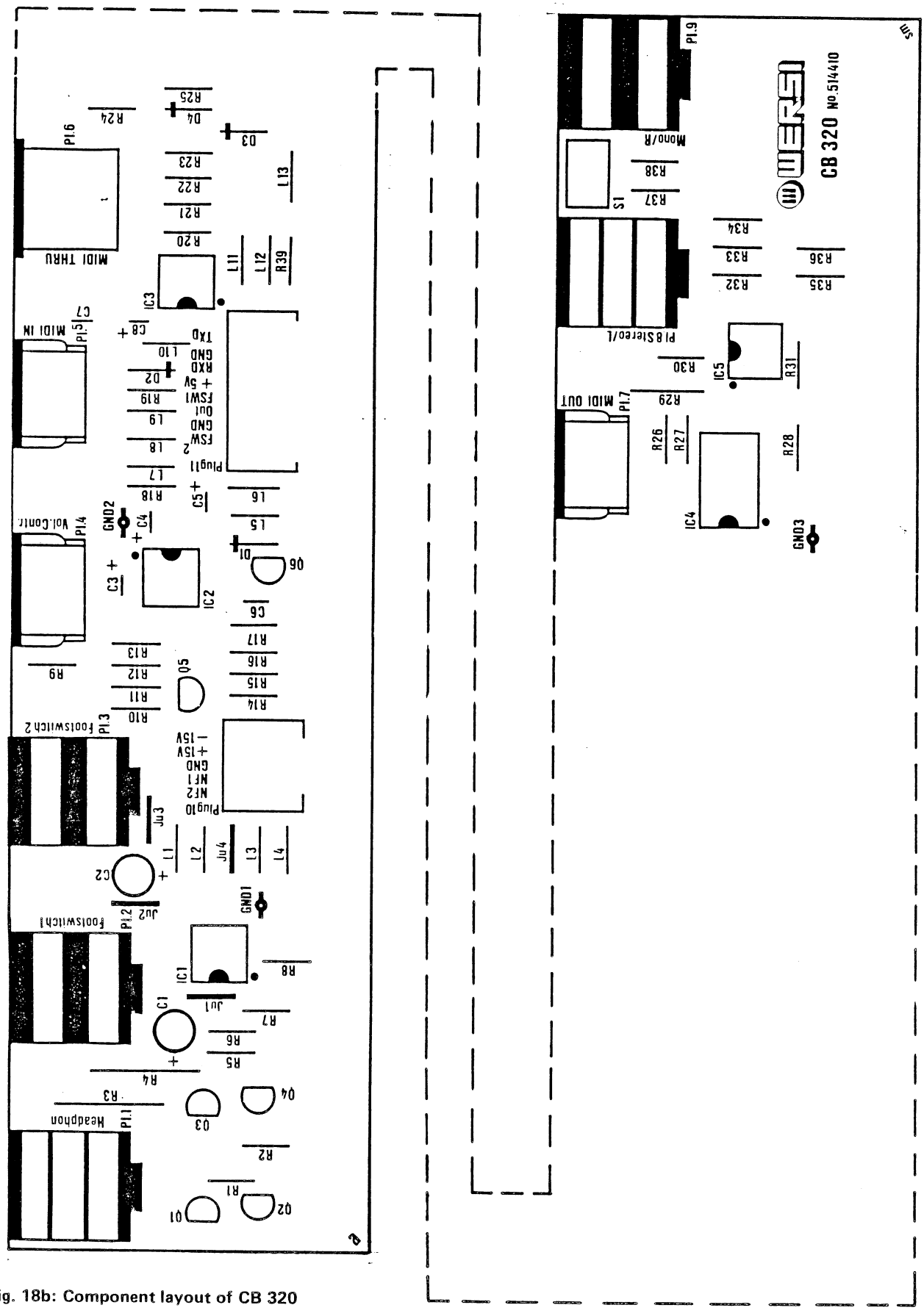


Fig. 18b: Component layout of CB 320

F. Technical Description of PC Board CBM 25 (only in OMEGA)

On PC board CBM 35 the signals of the 2 touch sensors (CB 29) are processed.

The touch sensors emit a voltage as a function of the pressure (on the manual). IC 1 (TLC 271) is wired as an impedance transformer and has a computed input impedance of about 15 GOhm!

On the shielded leads from the sensor, the shield is therefore not connected with ground but rather with the output of the amplifier (amplification = 1, that is, input voltage = output voltage), in order to eliminate loss in the cable.

R 1 (150 MOhm) and Q 1 cause the input to be pulled to 0 V with a large time constant.

Output voltage at "OUT" ranges from 0 V (no pressure on the manual) to about +4 V.

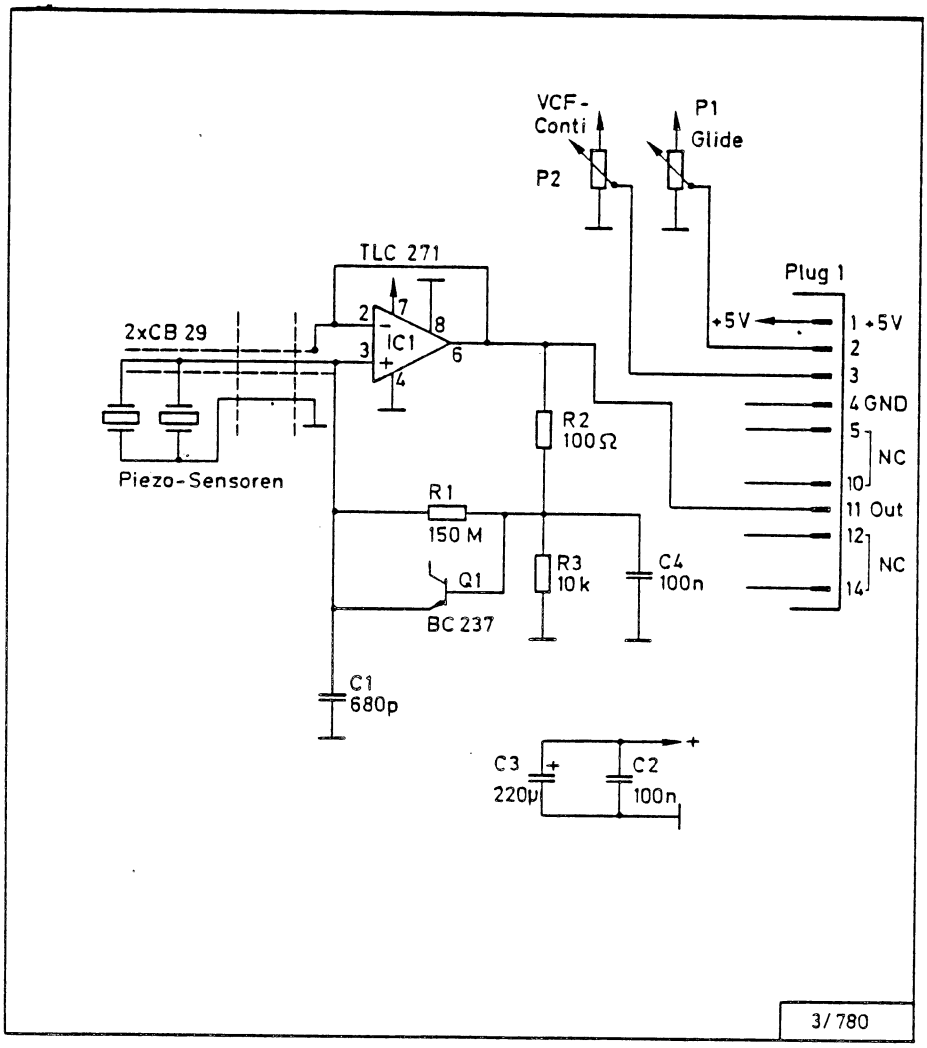


Fig. 19: Partial circuit diagram of PC board CBM 25

G. Technical Description of PC Board MM 1

1) Main Processor

This segment shows the basic elements of the main processor system: the CPU with its data bus driver (IC 16) and address bus buffer (IC 19, only for addresses Ø...7; A 8...A 15 are not buffered), the 32 kbyte program ROM (IC 3), the working RAM (IC 4) and the 3 memories for the voice data: (IC 5, the voice ROM, in which the 20 DMS voices are permanently stored (16 kbyte), and IC 1 and IC 2, each containing 10 CVs and 8 presets (2 x 8 kbyte-RAM). Together with the cartridge we have 3 memory blocks of 16 kbyte each, which controlled by the voice bank latch (IC 11) and the gates of IC 9 and IC 13, occupy a fixed address region of the CPU in banks.

The timer unit 68 B 40 (IC 6) is responsible for the timing. It contains 3 separate timer elements; with timer 1 generating 1 ms interrupts at the IRQ-pin for the master CPU, timer 2 providing the baud rate clock for the serial interface (IC 7) (at MIDI: 500 kHz), and timer 3 providing the co-processor with a 5 ms cycle in a different keying ratio which is inverted by Q1. In order to read and write synchronously, the R/W signal is connected to the 2 MHz clock E (IC's 9 and 13 at left of page) generating signals RD and WR. Since the system clocks are also needed in negative logic, E and Q are generated in 2 inverters (IC 40). Also shown are the connectors for the operating panels (plug 1), the analog card (plug 4) and the power supply (plug 3). Plug 5 is used only in organ model DX 10.

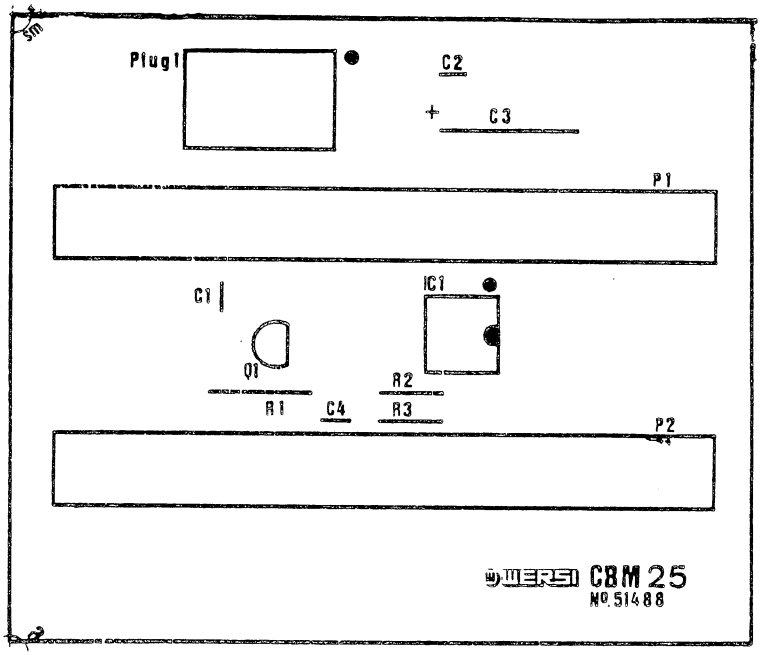


Fig. 20: Component layout of CBM 25

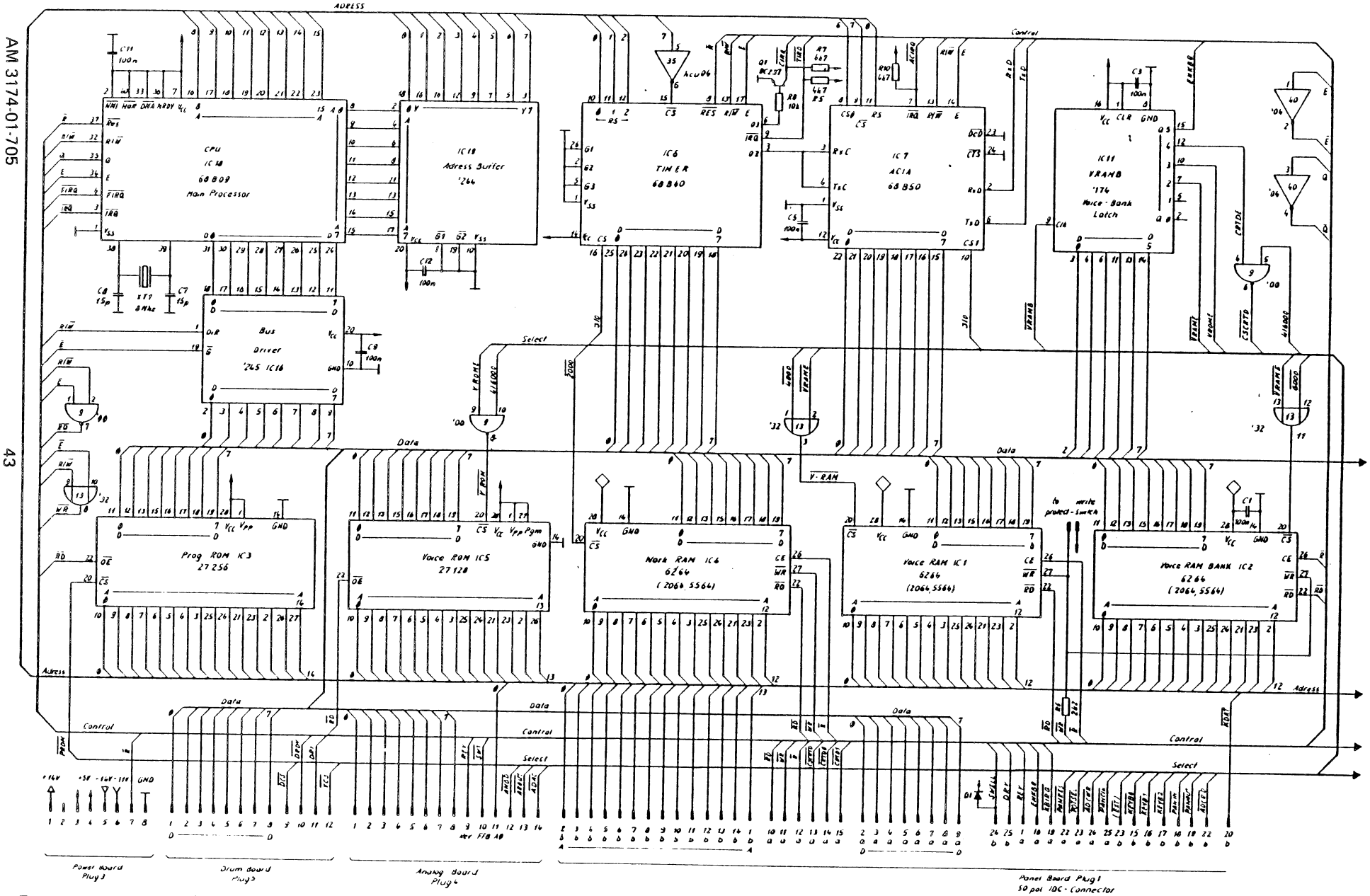


Fig. 21: Partial circuit diagram of MM 1 — Main processor

2) Decoding Section

In this section the address range of the main CPU is divided into the selects of the individual units. For details see the memory map charts on page 62.

The region to the upper left illustrates the interrupt control. For quicker recognition of all incoming interrupt signals, they are connected with a port unit, so the CPU can immediately determine the source of an interrupt by reading this port. These sources can be:

- Slave – IRQ
- Timer – IRQ
- Keyboard – Fast – IRQ (FIRQ)
- ACIA – FIRQ

Also connected to this port is the cartridge coding (CRTD Ø, CRTD 1) for recognizing whether ROM, RAM or no cartridge is inserted and the 2 foot switches (SW Ø, SW 1) are connected. (DRDY is not taken into account.)

A battery, which is constantly recharged while the unit is on, ensures that all memories will maintain their content after the unit is switched off. In the fully charged state, the battery will power all RAMs for several months.

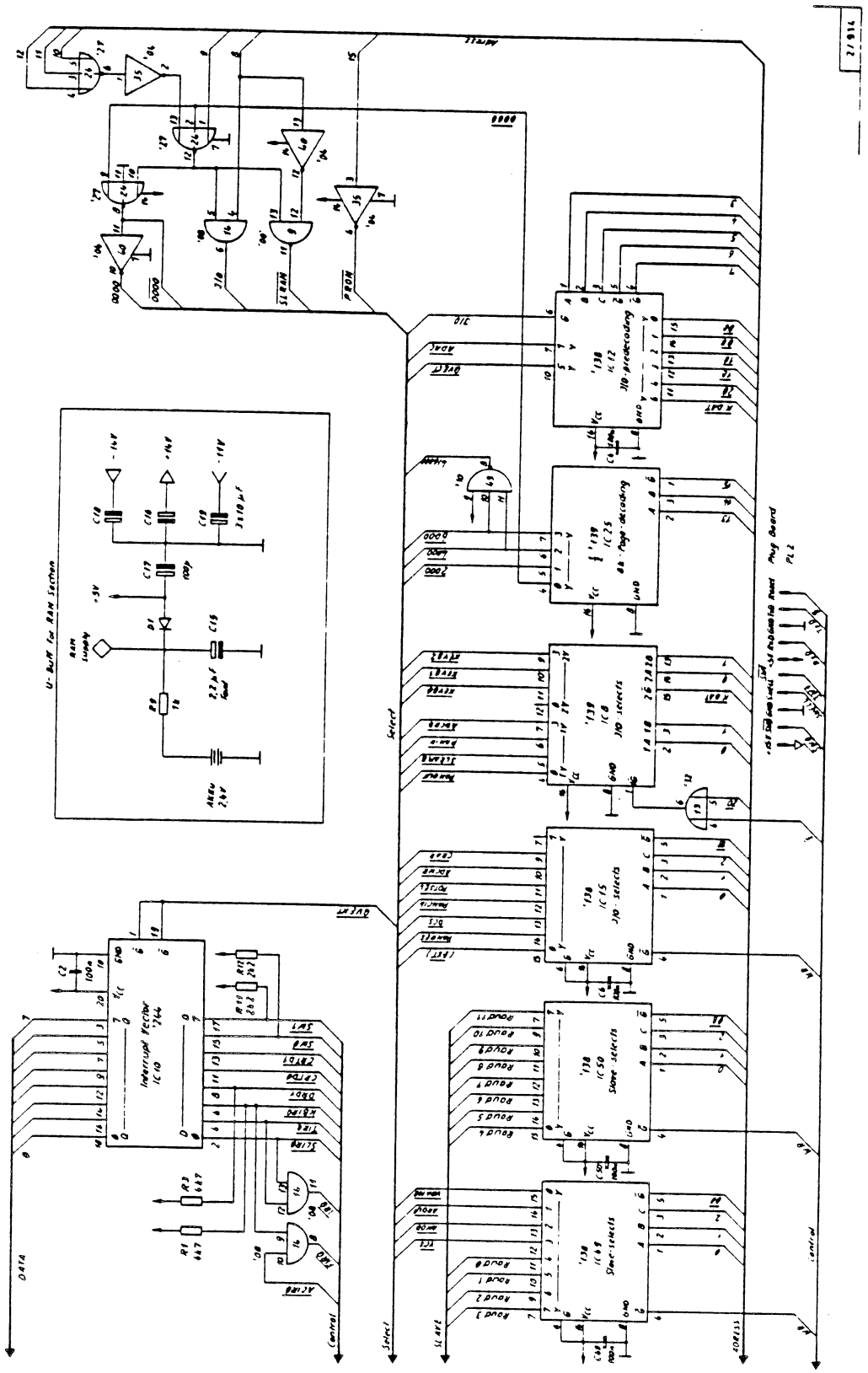


Fig. 22: Partial circuit diagram of PC board MM 1 - Decoding section

3) Co-Processor

The co-processor, model 68 B 09 E (IC 42) is supplied with the 2 MHz clock (E, Q) that is shifted one-half clock cycle relative to the master CPU 68-B 09. Since the processors of this family have the characteristic of accessing the system only during half the clock period, both processors can read or write the communications RAM (IC 26) "simultaneously." The address bus and data buses are alternately switched to the RAM in the CPU cycle (E). For the address bus and the control signals $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$, IC 20 through IC 23 perform the switching; for the data bus this is done by IC 36 and IC 38.

The co-processor calculates the amplitude for a maximum of 20 slaves and outputs it synchronously with the frequency envelope of the corresponding voice. The envelope output is the domain of the D/A converter DAC 1232 (IC 27), which on the output side of R 14, outputs the analog envelope with a resolution of 12 bits and multiplexed for 20 channels with a voltage ranging from 0 to -10 V. (P 1 is used for adjustment of exactly 0.000 V with the voice switched off). Then the signal is separated into individual signals via demultiplexers IC 44 and IC 45 (also extension card IC 3) and fed to the sample and hold stages IC 46, 47, 48 (MME: IC 1, 2), which then feed individual voice cards. IC 37 and IC 39 are responsible for addressing a signal and hold channel. The envelope clock signals of 5 ms (ECLK Ø. . .19) are produced separately for each slave (IC 41; MME 1; IC 5) to ensure synchronization of the frequency envelope and the amplitude envelope.

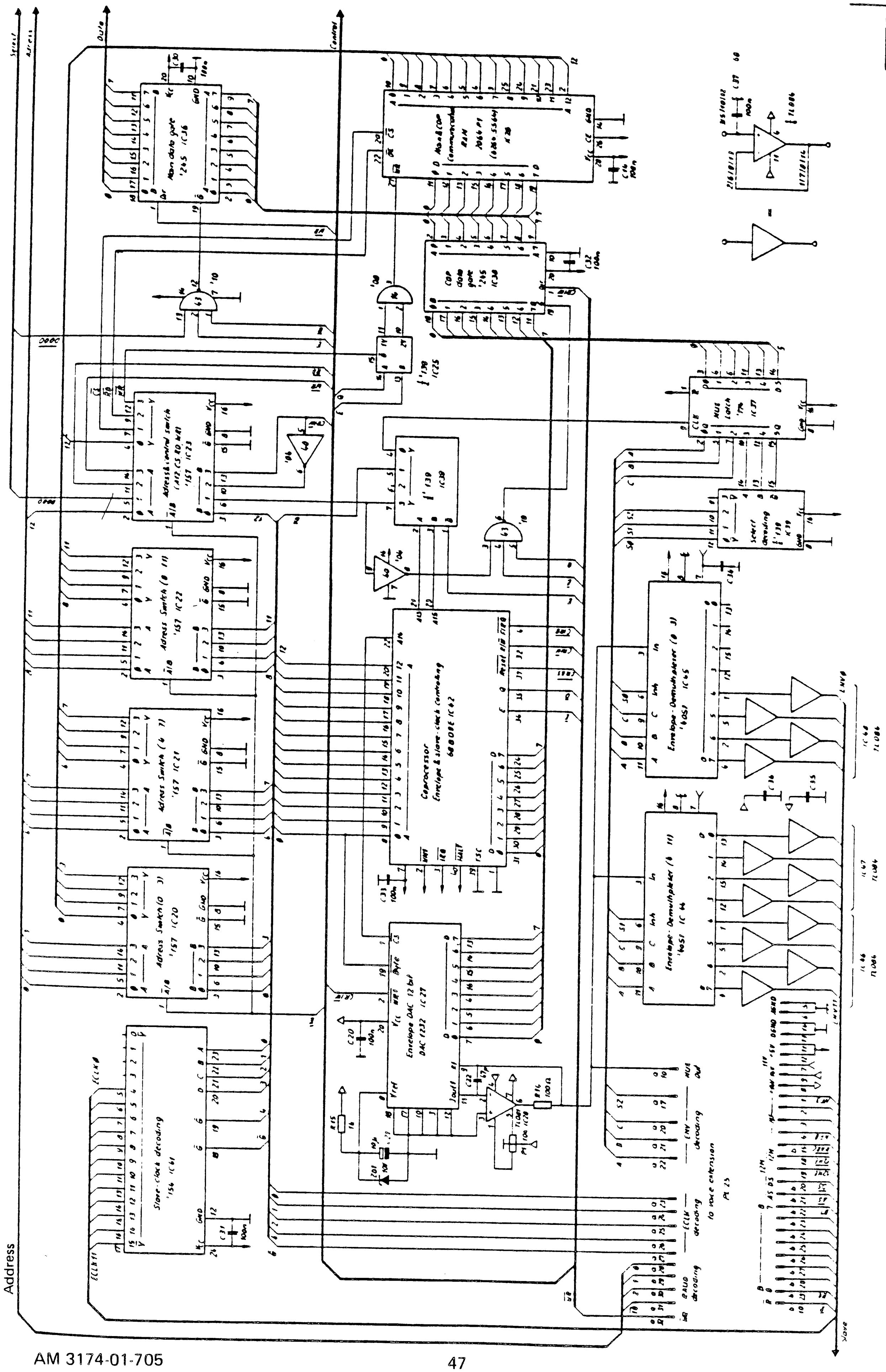


Fig. 23: Partial circuit diagram of PC board MM 1 - Co-processor

4) Slave Section

This section illustrates the connection between the master processor system and the slave cards. The master writes all necessary data concerning frequency envelope, wave shape, routing sound frequency and pitch into the slave RAM (IC 31) via buffers IC 32 and IC 30. However, since only 256 byte blocks are available (the slave processors can no longer address!), the 8 kbyte RAM is divided into 32 segments. IC 17 is responsible for this banking. Since each sound component needs 1 segment, 8 groups of up to 4 components each can be provided (also 8 MIDI channels simultaneously!).

Once the master CPU has accessed the slave RAM, the slave RAM control flip-flop (IC 34) switches the master bus system to this RAM (through IC 33) and thereby simultaneously signals to the slave processors that they may not perform any bus accessing to the RAM ($\overline{RARC}$ = low). When the master has concluded the parameter transmission to the slave RAM, it releases the latter for accessing by resetting the flip-flop with $\overline{CRAR}$, and the control buffer IC 33 goes to high resistance (3-state). The respective slave, with the address line $\overline{RAUD}$ (IC 49, 50, MME, IC 4), is then operated and gathers the data in the RAM. Since it transmits the addresses and data over the same bus lines (B Ø. . .B 7), the address byte is interim-stored in the address latch IC 29. Even during this process, it reports its response to the slave RAM by low-switching the $\overline{RARC}$ line.

After the data transfer is concluded, the slave ready unit (IC 34) generates an interrupt at the main CPU (SLIRQ) and writes the value FF (hex) into the address latch. The content of this address, together with the 2 exponent lines EXSLA Ø and EXSLA 1, yields the actual pitch value, which has validity if no other bus accessing occurs ($\overline{RARC}$ = high).

The 12 MHz clocks of opposite phase needed for the slave timing are generated by the inverter of the IC 35 and buffered in IC 33.

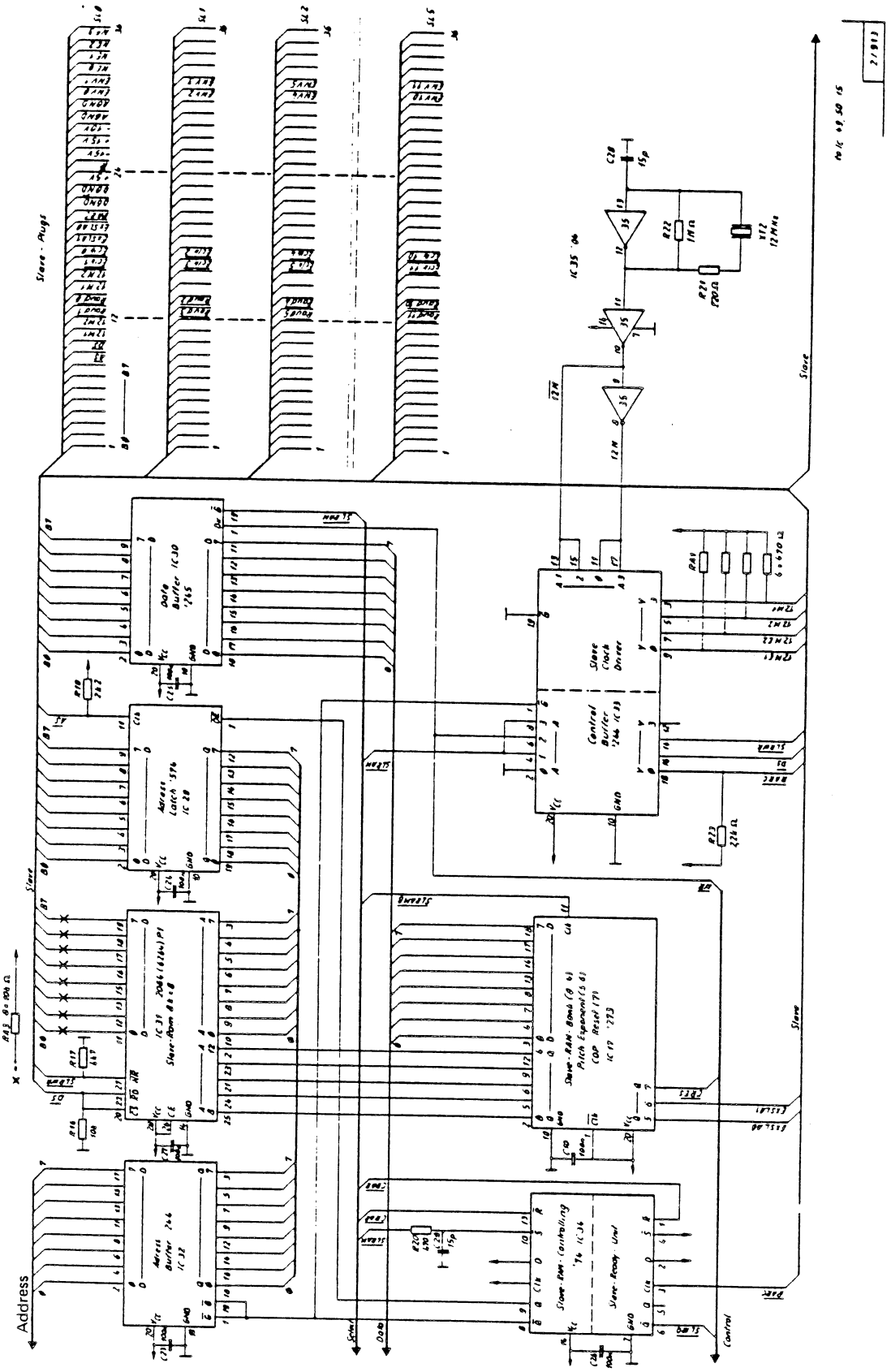


Fig. 24: Partial circuit diagram of PC board MM 1 - Slave section

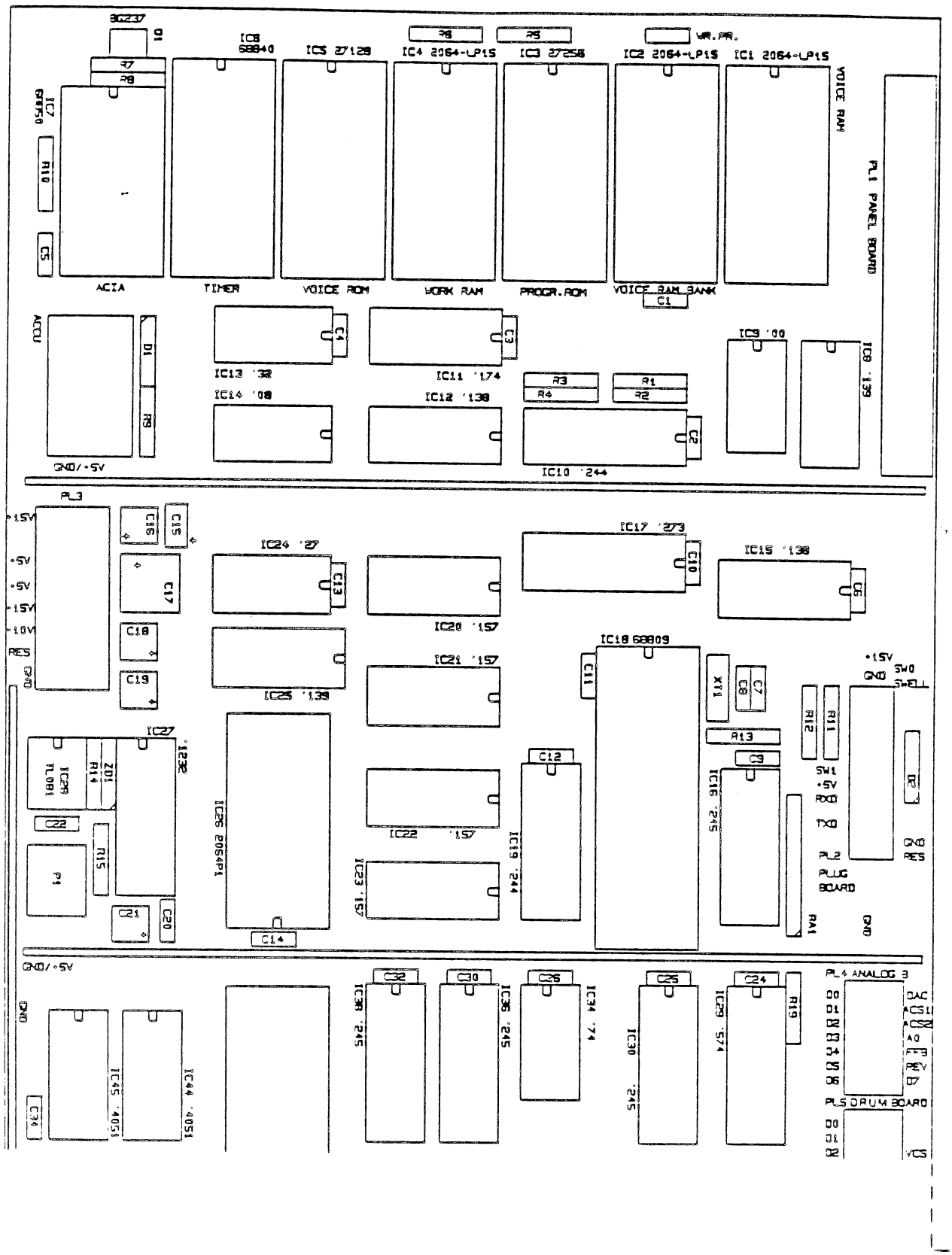
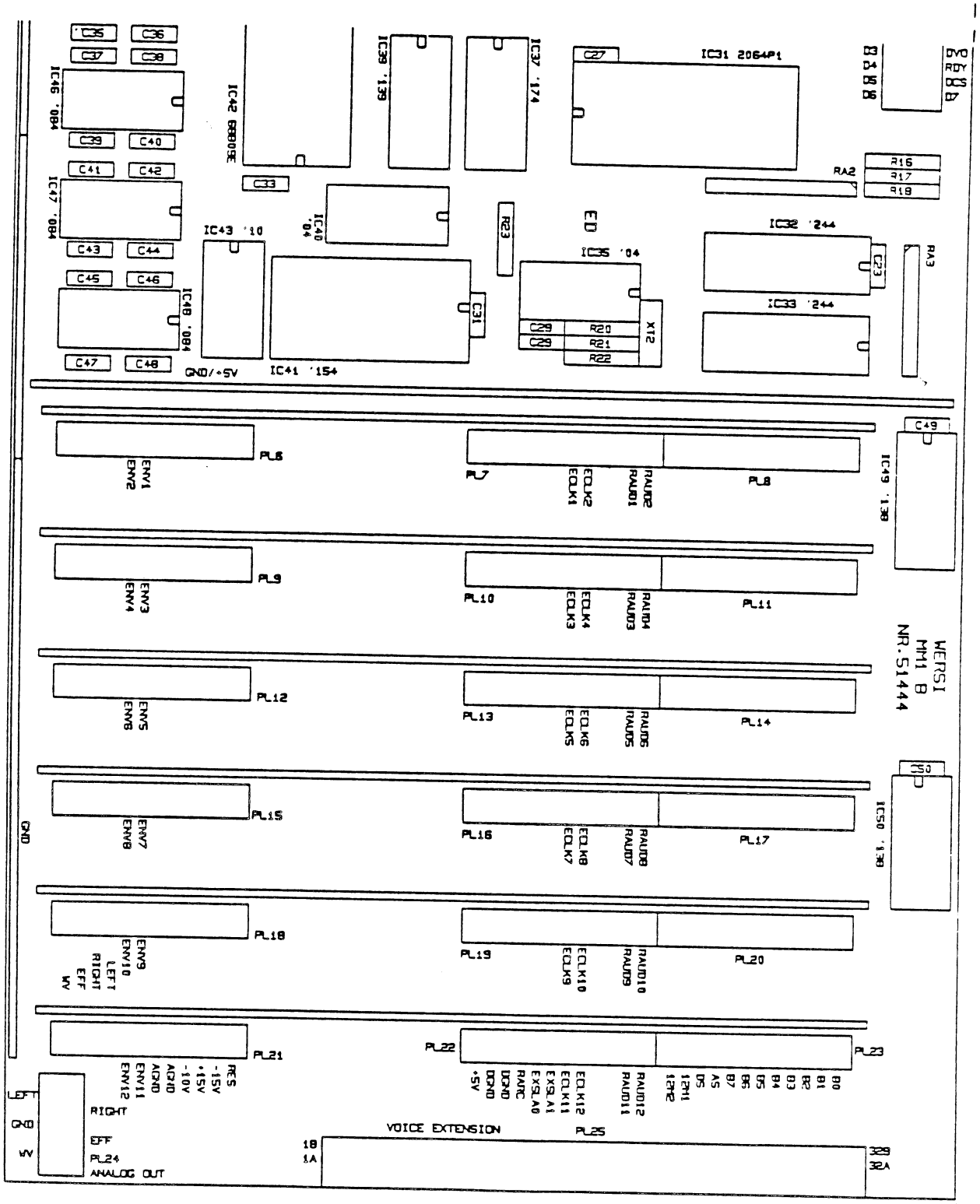


Fig. 25: Component layout of PC board MM 1


C35
C36
C37
C38
IC46 '084
C39
C40
C41
C42
IC47 '084
C43
C44
C45
C46
IC48 '084
C47
C48
IC42 68B09E
C33
IC43 '10
GND/+5V
IC41 '154
IC40 '04
C31
IC36 '139
IC37 '174
C27
IC31 2064P1
R23
IC35 '04
C29
C29
R20
R21
R22
X12
RA2
R16
R17
R18
IC32 '244
IC33 '244
C23
RA3
C49
IC49 '138
C50
IC50 '138
PL6
ENV1
ENV2
PL7
ECLK2
ECLK1
RAUD2
RAUD1
PL8
PL9
ENV3
ENV4
PL10
ECLK4
ECLK3
RAUD4
RAUD3
PL11
PL12
ENV5
ENV6
PL13
ECLK6
ECLK5
RAUD6
RAUD5
PL14
PL15
ENV7
ENV8
PL16
ECLK8
ECLK7
RAUD8
RAUD7
PL17
PL18
ENV9
ENV10
LEFT
RIGHT
EFF
WV
PL19
ECLK10
ECLK9
RAUD10
RAUD9
PL20
PL21
ENV11
ENV12
AGND
AGND
-10V
+15V
-15V
RES
PL22
+5V
DGND
DGND
RAMC
EXSLA0
EXSLA1
ECLK11
ECLK12
RAUD12
RAUD11
PL23
12M2
12M1
A5
D5
B7
B6
B5
B4
B3
B2
B1
B0
VOICE EXTENSION
PL25
18
1A
32B
32A
LEFT
GND
WV
RIGHT
EFF
PL24
ANALOG OUT
GND
WERSI
MM1 B
NR.51444

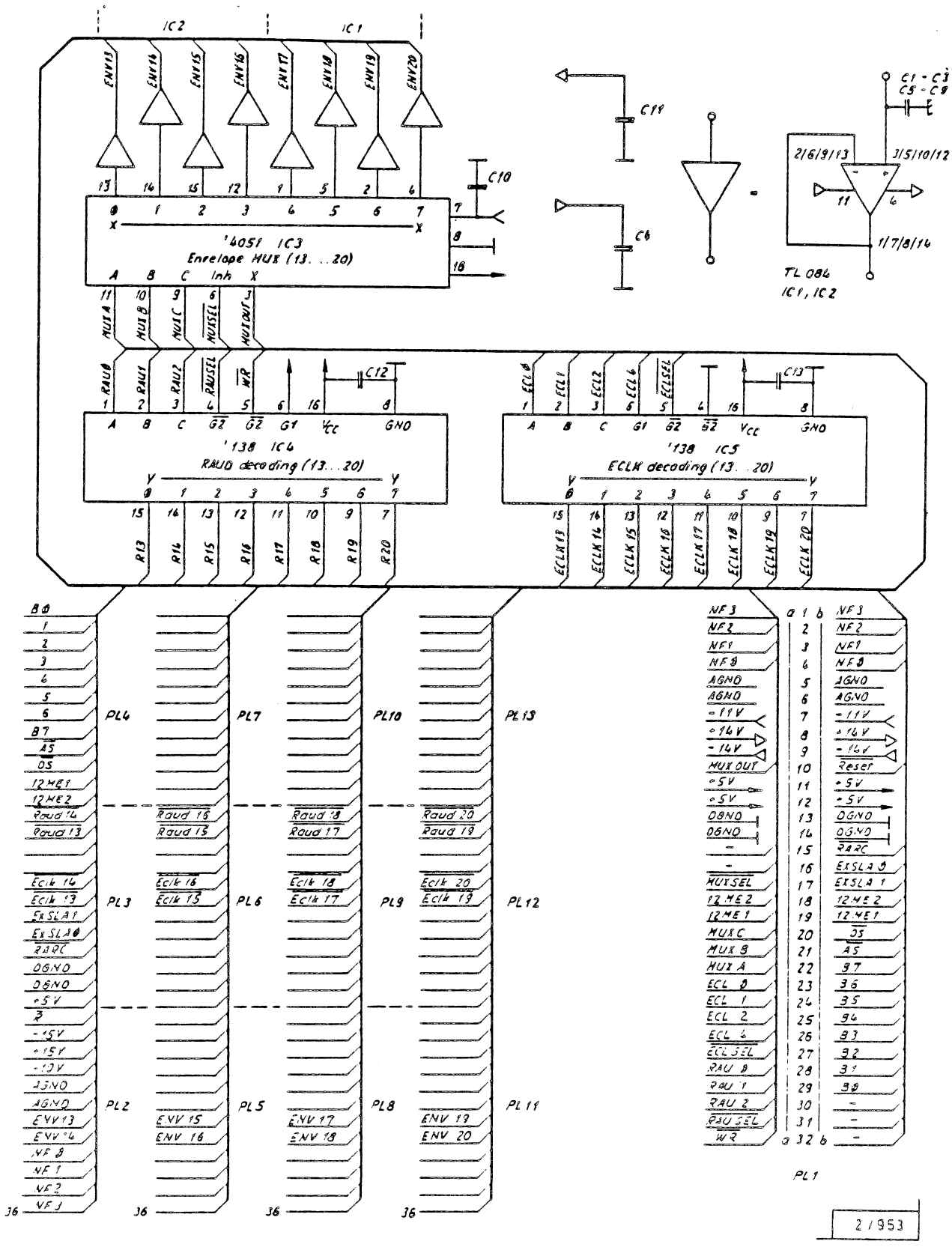


Fig. 26: Circuit diagram of PC board MME 1

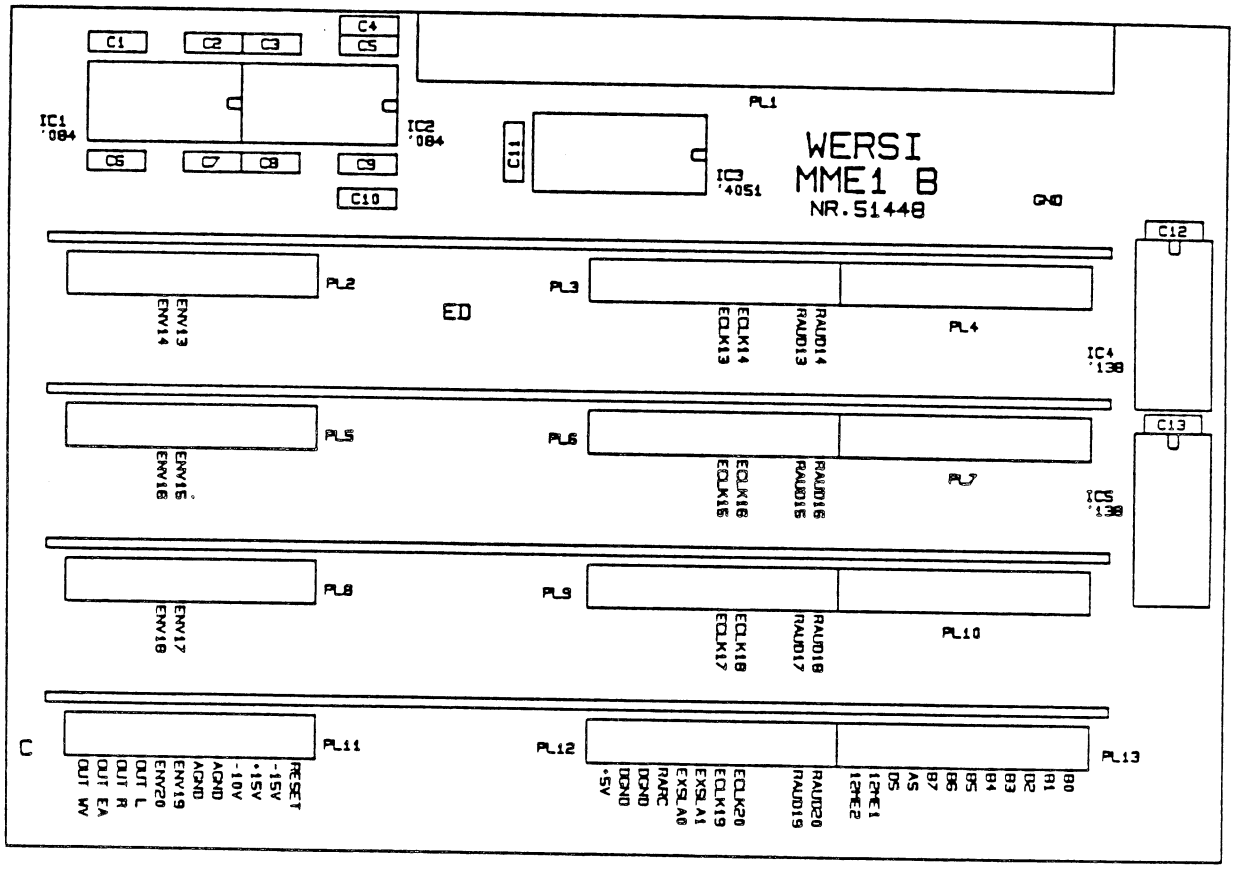


Fig. 27: Component layout of PC board MME 1

H. Technical Description of PC Board SL-M2

PC board SL-M2 contains 2 identical sound generating modules which are capable of outputting a wave shape with a fixed or on-line formant nature including a very complex frequency envelope. The heart of this sound generation is a single chip microcomputer. This component is controlled via the data communication which it maintains with the slave RAM via its port 1 (IC 9, 10: pin 21...28). This port is switched as a multiplexed address data bus during the data transfer and is otherwise an input port. The bus control lines $\overline{AS}$ and $\overline{DS}$ can be high-impedance switched through the microprocessor itself with the aid of the 3-state driver IC 7. The meaning of the signals $\overline{RAUD}$, $\overline{ECLK}$, EXSLA and $\overline{RARC}$ is explained in the slave and co-processor portions of the master description. The wave shape output is through port Ø (pin 13...20) in the double-stage-buffered 8 bit D/A converter DAC 0832 (IC 6, 8). However, the value travels synchronously with the internal timer of the microprocessor to the output. These timer slopes are prepared in advance with the exclusive-OR gate 4070 (IC 5) to pulses of constant length.

As a reference, the DAC receives the amplitude envelope voltage (ENV) generated by the co-processor. The 200 Hz timing frequency is filtered out with the RC combination 1 kOhm, 2.2 uF. The diodes provide for a rapid rise and fall of the envelope. The sound signal then travels to the second operational amplifier, which then optionally carries out an 80 Hz low pass (bright) via IC 3. Finally, the audio path through the 4 possible audio multi-bus circuits is determined via the output routing switch (IC 1, 2). As we see, there are only 8 possibilities for the routing combination:

- left
- right
- effects
- Wersivoice (WV)
- left + right
- right + effects
- left + WV
- WV + effects

This switch corresponds to the direct routing voice in its operation.

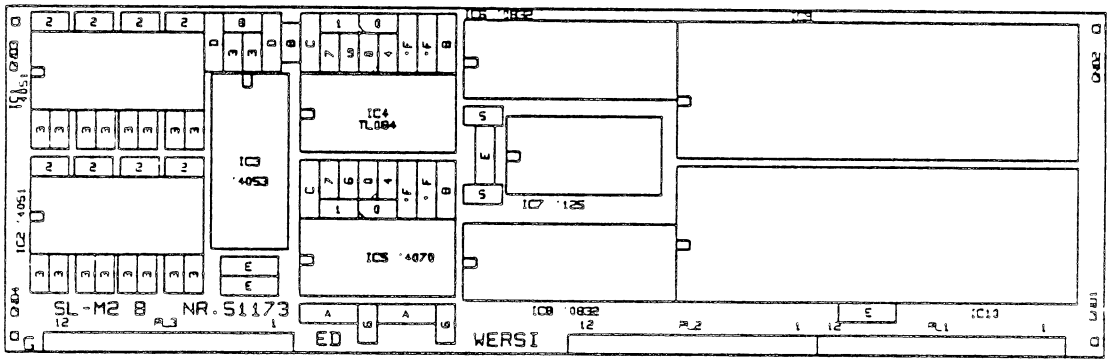


Fig. 28: Component layout of PC board SL-M 2

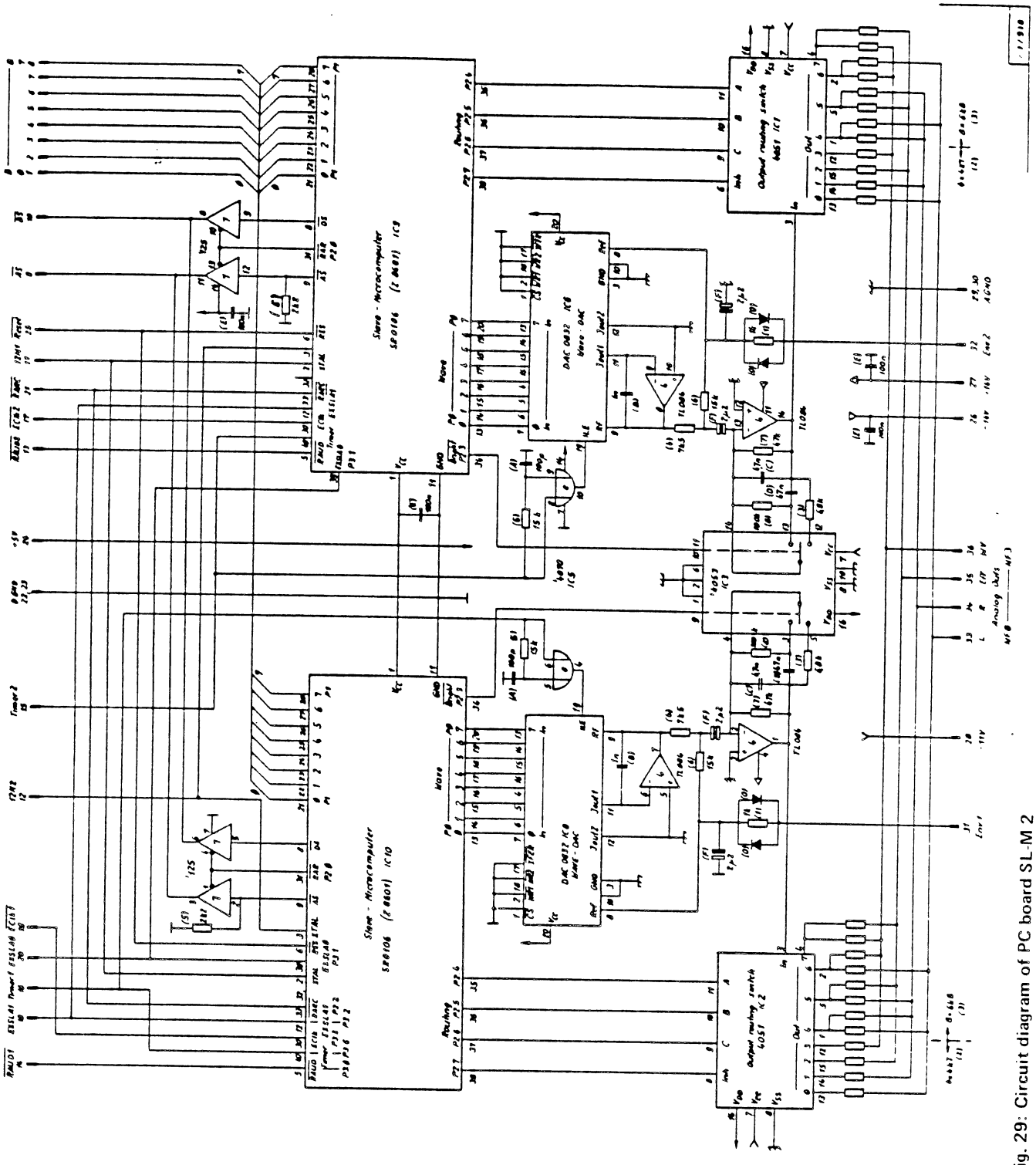


Fig. 29: Circuit diagram of PC board SL-M 2

I. Technical Description of PC Board AF 20 or AF 21

In PC board AF 20 (later models, AF 21), the analog processing of all audio signals arriving from the exterior is done by the DX 10 itself. The so-called routing, that is, the coordination according to channels and the further transmission, is determined by the software.

Let us first examine the block diagram (Fig. 30). The slaves (PC boards SL-M2) indicated at the extreme left have internal software-control routing switches by which up to 4 different audio signals are provided at the slave outputs:

1. Direct signal, left
2. Direct signal, right
3. WV signal
4. VCF signal

These 4 signals are then received by the input amplifier stages of PC board AF 20/21 and processed as follows:

The 2 direct signals – hence their names – are transmitted directly to the volume control stages VOL (software-controlled as a function of the volume pedal) then via the noise suppression stage DYNAFEX^{R} and the relay to outputs AF/L (left) and AF/R (right).

The WV signal ("WV" stands for WERSIVOICE) passes through the block of the same name, which causes various modulations (string, vibrato or choir effects) and travels to the 2 direct channels, where it is further processed together with the direct signal.

Depending on the setting of the analog switch S 2, the last of the 4 slave signals – VCF – travels directly or via a distortion stage to the VCF stage (tunable filter), then – depending on S 3 and S 4 – either to the Wersivoice or to the direct channel (routing over both pathways is also possible). The stage NOISE is an additional white-noise generator.

After all SLAVE signals are passed through the volume control stage VOL, part of the signal is branched off from 2 channels L and R and transmitted to the reverb input amplifier, which supplies the actual reverb unit. The reverb signal returning from there is again added to the original signals via the stage VOL. REV.

At the same place, the signals coming from the rhythm unit are further processed either directly or via the reverb branch. Microphone or taped signals would also be added here.

Shown to the far right in the block diagram is the interface between the main processor (MM 1) and the analog PC board (AF 20/21). After cyclic interrogation of the volume pedal, wheels, touch and all shift registers (Fig. 8 – CBM 30), their momentary values are converted to digital information for the processor and again converted to corresponding analog control signals in the DAC and the multiplexer.

Circuit Diagram AF 20 (Figs. 31a): at the upper left and right we see the 4 input amplifiers IC 1 (the IC numbers are circled) for the slave signals which "come in" via PL 3, connections 1 through 4. The so-called direct signals (1 and 2) travel to the IC 1 amplifiers shown at the top right; WV and VCF signals (3 and 4) travel to those shown at the top left. All signals ultimately pass through the intermediate amplifier IC 2 to the current-controlled volume control stages IC 3. The control currents needed at the control inputs 1 and 16 of the IC 3 are supplied by transistors Q 1 and Q 2, respectively, which in turn receive their information on IC 25 from the multiplexer IC 27, pin X 7, and lastly, via IC 25 (D/A converter) from the main processor.

The Wersivoice block is made up of ICs 28 through 33; the necessary control voltages for modulation are supplied by the main processor.

In the VCF region, IC 5 (1/2), brings about the aforementioned distortion; IC 14 provides the noise, and the actual VCF filter is made up of the ICs 7 through 10; the "heart" is the IC 9 operating on the principle of the capacitor switching.

The analog switches (S 1 through S 4) in the block diagram consist of ICs 11 and 12; 3 such switches are housed in each IC.

Technical Description AF 21 (Fig. 31b)

The audio signals enter the AF 21 from the MM 1 via PL 2 (found in upper left corner of schematic) and are amplified by the four stages of IC 24 (IC numbers are circled).

The Wersivoice (WV) input signal is compressed by IC 22 and travels through IC 6 (low-pass filter) to the input of the "bucket brigade" circuit, consisting of IC's 12, 13 and 15 with associated circuitry. The delay and phasing of the audio signal in each "bucket brigade" IC is determined by the clock received from IC's 3, 4 and 5, which are Voltage Controlled Oscillators (VCO). The VCO's receive a varying DC voltage (WV1, WV2, WV3) from IC 16. The three delayed audio signals (output of IC's 12, 13 and 15) are summed at IC 14, travel through IC 6 (low-pass filter) and is decompressed by the 2nd half of IC 22, returning the signal to its original levels.

The VCF (Voltage Controlled Filter) input signal goes through IC 24 to IC 25, where it can be switched directly to VCF IC 18 or through the distortion stage of IC 17 and 18. The actual filtering is done by IC 18 with it receiving external control information via pins 5 and 17. The VCF output can be switched to either a 12 dB/octave or 24 dB/octave low-pass filter at IC 25 and IC 17. At IC 19, the signal can be switched to the left or right channel or onto the WV.

All output signals from the WV, VCF and those coming in directly from MM 1 on left and right channel are summed at IC 20 and fed into VCA (Voltage Controlled Amplifier) IC 27. The voltage at pins 5 and 10 determine the output level (TP 25 = 0, no output; TP 25 = +2V, full volume). This voltage is determined by the swell pedal.

The IC 27 output is summed with signals from the reverb, rhythm and microphone input at IC 26, which gives the signals final amplification (preamp) before being sent to the output via PL 6.

The reverb signals are summed at IC 6, pin 2, and fed to the DH 10 board via PL 11. The processed reverb signals (right and left) return via PL 11 through IC 28 to the VCA IC 29, which works as IC 27 (previously explained) for controlling the reverb volume.

All control information is controlled by the master processor on MM 1 and comes onto AF 21 via PL 1. IC's 7 and 8 latch and hold the information for analog switch IC's 19, 21 and 25. Other control voltages are developed by IC 1 (Digital/Analog Converter) and demultiplexer by IC 10. Each signal then received filtering at IC's 16 and 23.

Test Points

For the purpose of following signals and to assist in troubleshooting, important Test Points are marked as TP. Please note that some signals (like those for analog switches) are only present while a key is pressed or for as long as the tone is being generated.

Following is a list of test points.

TESTPOINT TP . . . ON AF 21

TP NAME	EXPLANATION	VOLTAGE READING
01. Env. Dist	Distortion volume control voltage — This voltage is controlled by the volume control for the keyboard in use.	0 . . + 10 V
02. Env. Delay 1 03. Env. Delay 2 04. Env. Delay 3	Modulation voltages for the three bucket brigade circuits	Accord. to the selected mode (0 . 5 . . 7 Hz) 0 . . + 10 V
05. Env. VCF, Frequency 06. Env. VCF, Quality	Control voltage for the VCF-frequency Control voltage for the VCF-bandwidth (quality)	Approx. 1 V/Octave 0 V = Value of After approx. + 6 V Oscillation
07. Env. Noise	Noise, Envelope	0 . . + 10 V
08. Env. Volume	Master Volume — Controlled by Master Volume Control and/or Volume Pedal	0 . . + 10 V
09. DAC: Out	Multiplexed DAC Output	0 . . + 10 V
10. WV, Compressor Out 11. Delay, In 12. Delay, Out 13. Delay, Out 1 14. Delay, Out 2	Compressed signal for WV Delay input for WV Delay output for WV Delay output from 1st filter stage Delay output from 2nd filter stage	Approx. 1 V_{ss} + 7.5 V Approx. 1 V_{ss} + 7.5 V Approx. 2 V_{ss}* Approx. 2 V_{ss}* Approx. 2 V_{ss}*
15. VCF, Out 16. WV, Out	VCF Output WV Output	Approx. 2 V_{ss}* Approx. 2 V_{ss}*
17. Left, In 18. Right, In 19. VCF, In 20. WV, In	Summed bus for each routing channel from slaves	Approx. 1.5 V_{ss}* Approx. 1.5 V_{ss}* Approx. 1 V_{ss}* Approx. 2 V_{ss}*
21. Sum. Left, Prefade 22. Sum. Right, Prefade	Summed output for Left/Right/WV/VCF/Ext.	Approx. 1 V_{ss}* Approx. 1 V_{ss}*
23. Sum. Left, Postfade 24. Sum. Right, Postfade	Like TP 21/22, but controlled by Master Volume	Approx. 40 mV_{ss}* Approx. 40 mV_{ss}*
25. VCA, Control 26. Reverb, Control	Control voltage for VCA — Same response as TP 8	0 . . 2 V 0 . . 2 V
27. Rhythm, Left 28. Rhythm, Right	Rhythm Input	
29. Out, Left 30. Out, Right	Audio Output	Approx. 4 V_{ss}* Approx. 4 V_{ss}*

NAME	EXPLANATION	VOLTAGE READING
31. Reverb, Left, Pref.	Reverb return input left	
32. Reverb, Right, Pref.	Reverb return input right	
33. Reverb, Left, Postf.	Reverb return input with volume control	
34. Reverb, Right, Postf.	Reverb return input with volume control	
35. Distortion, Out	Distortion Output	Approx. 1 V Level
36. Noise, Out, Postfade	Noise Output	0 . . + 10 V

*Test with 8' drawbar out, full chords, all volume control at full volumes. Different registration may give different voltage levels. What is most important, however, is comparing the voltage in relation to each other.

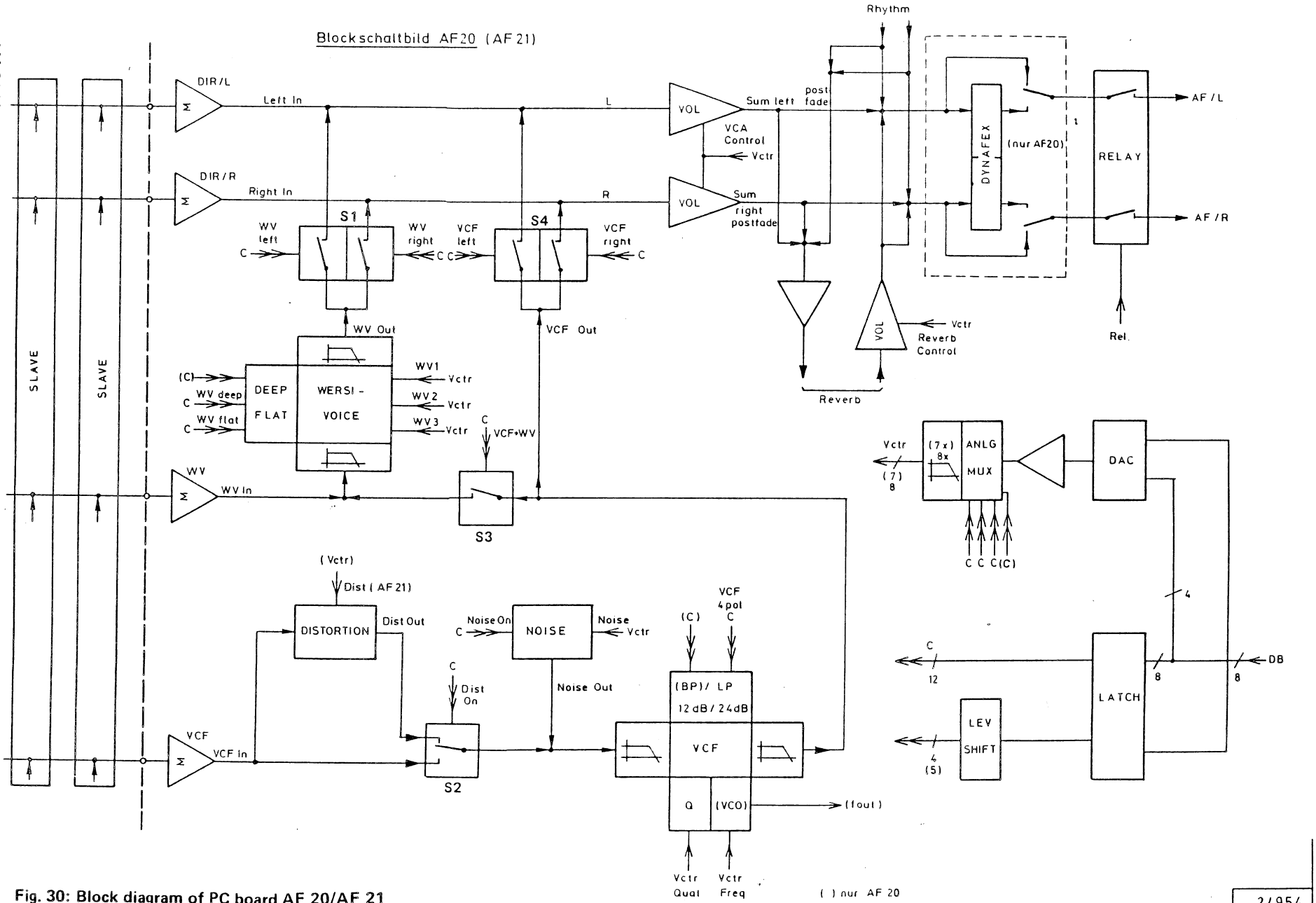


Fig. 30: Block diagram of PC board AF 20/AF 21

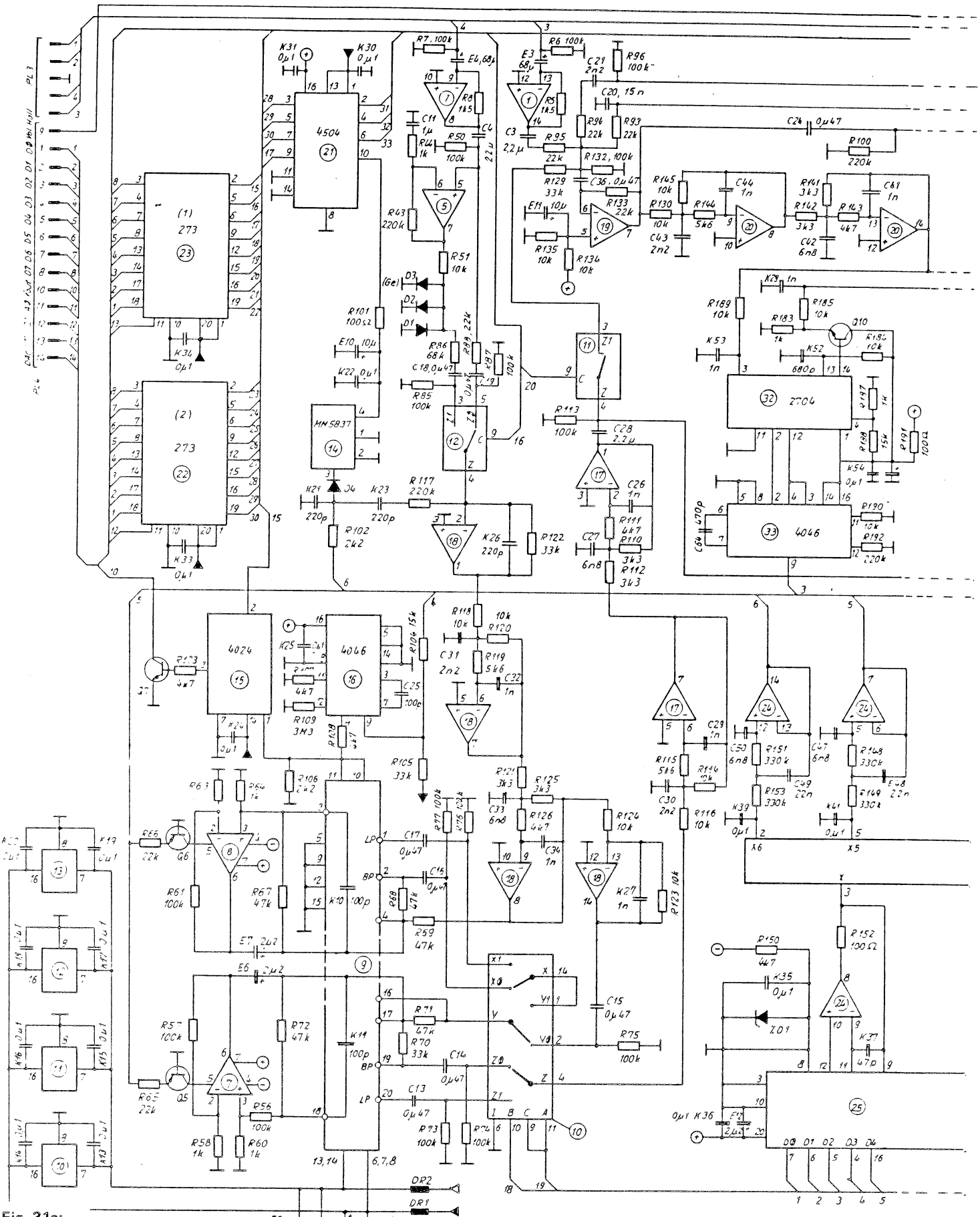
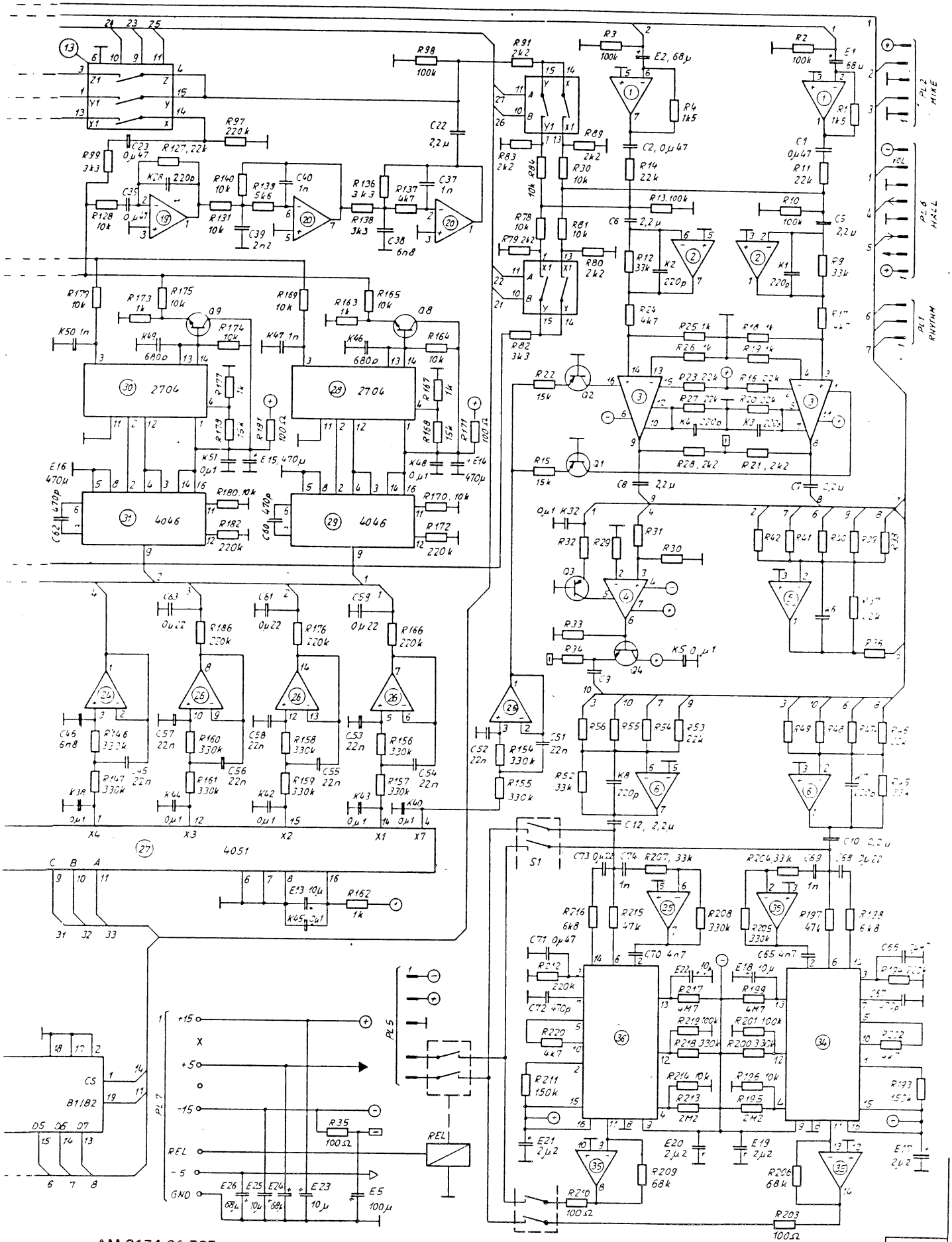


Fig. 31a:
Circuit diagram of PC board AF 20


4051
4046
4046
2704
2704
PL2 MIKE
PL0 HALL
PL1 RHYTHM
PL5
PL7
REL1
S1

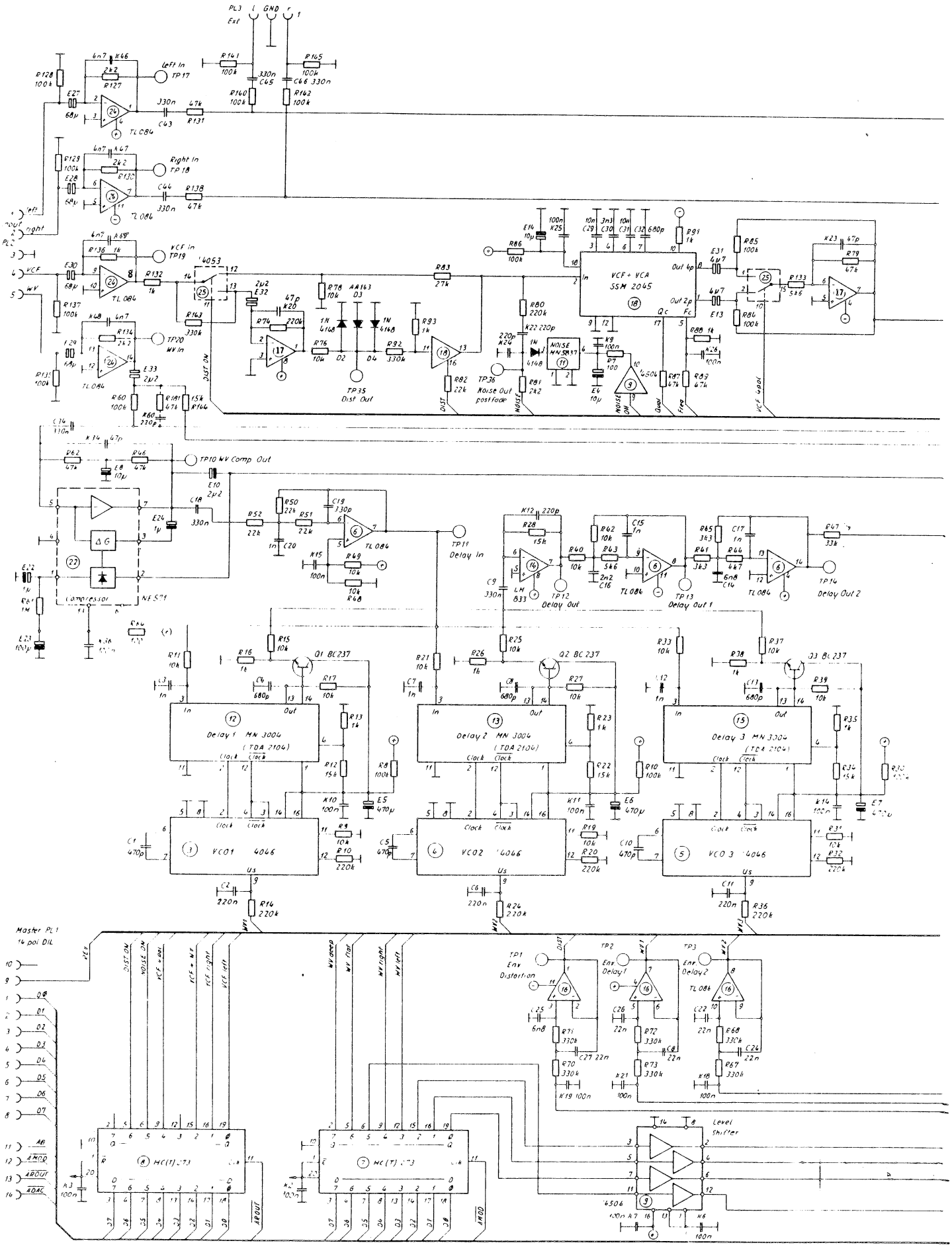
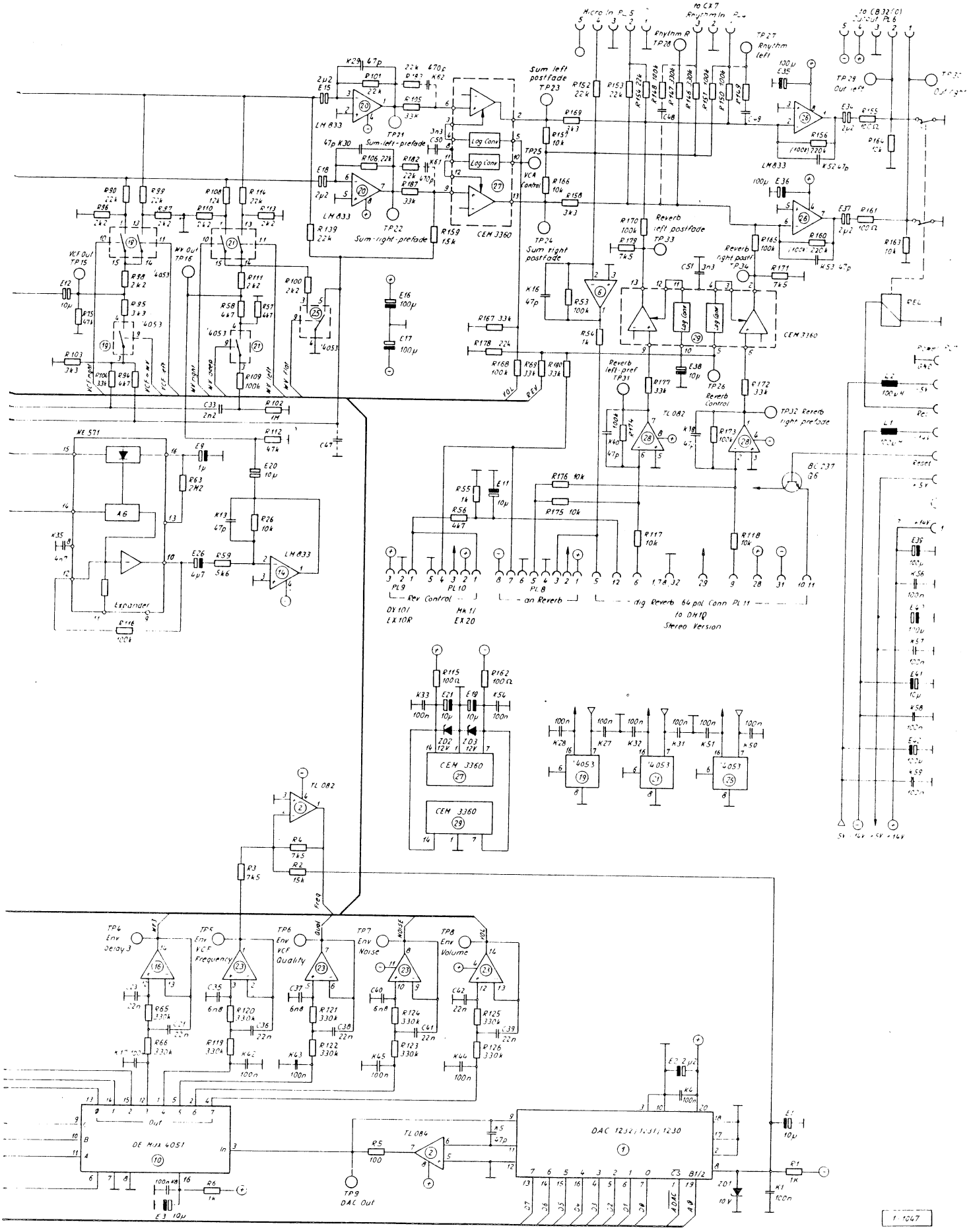


Fig. 31b: Circuit diagram of PC board AF 21

AM 3174-01-705

1/1047


Sum left postfade TP23
Sum-left-prefade TP21
Sum-right-prefade TP22
Sum right postfade TP24
VCA Control TP25
Reverb left postfade TP33
Reverb right postf TP34
Reverb left-pref TP31
Reverb Control TP26
TP32 Reverb right prefade
Rhythm R TP28
TP27 Rhythm left
TP29 Out left
TP30 Out right
Micro In P_5
to CX7 Rhythm In P_4
to CB32(C1) Output P_6
CEM 3360
LM833
TL082
TL084
BC 237
Expander
PL9 — Rev Control
PL10
PL8 — an Reverb
— dig Reverb 64 pol Conn PL11 —
to DM10 Stereo Version
DX 10/ EX 10R
MK 1/ EX 20
TP4 Env Delay 3
TP5 Env VCF Frequency
TP6 Env VCF Quality
TP7 Env Noise
TP8 Env Volume
OE MUX 4051
DAC 1232/1231/1230
TP9 DAC Out
Reset
+5V
+14V
-5V
-14V

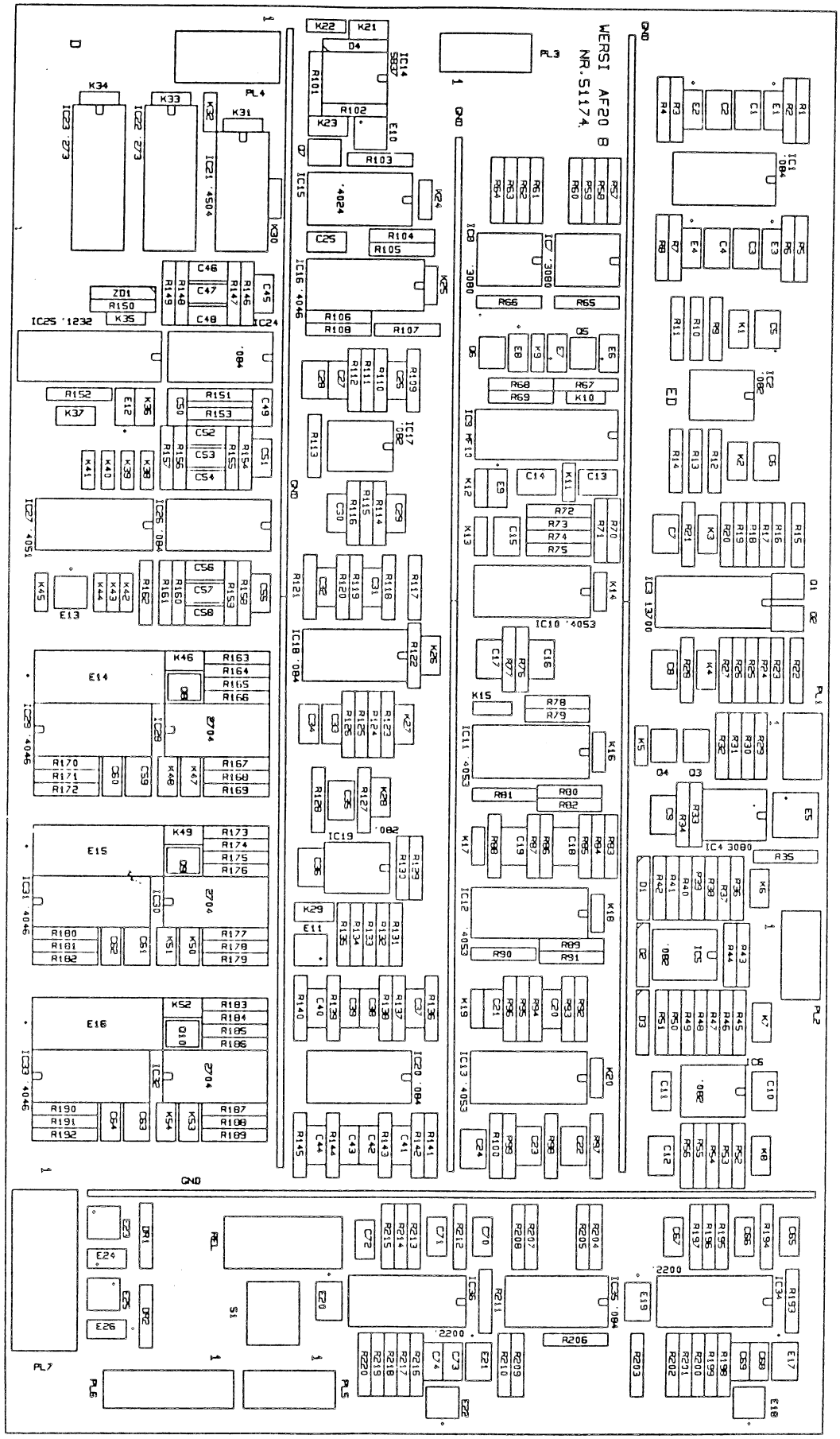


Fig. 32a: Component layout of PC board AF 20

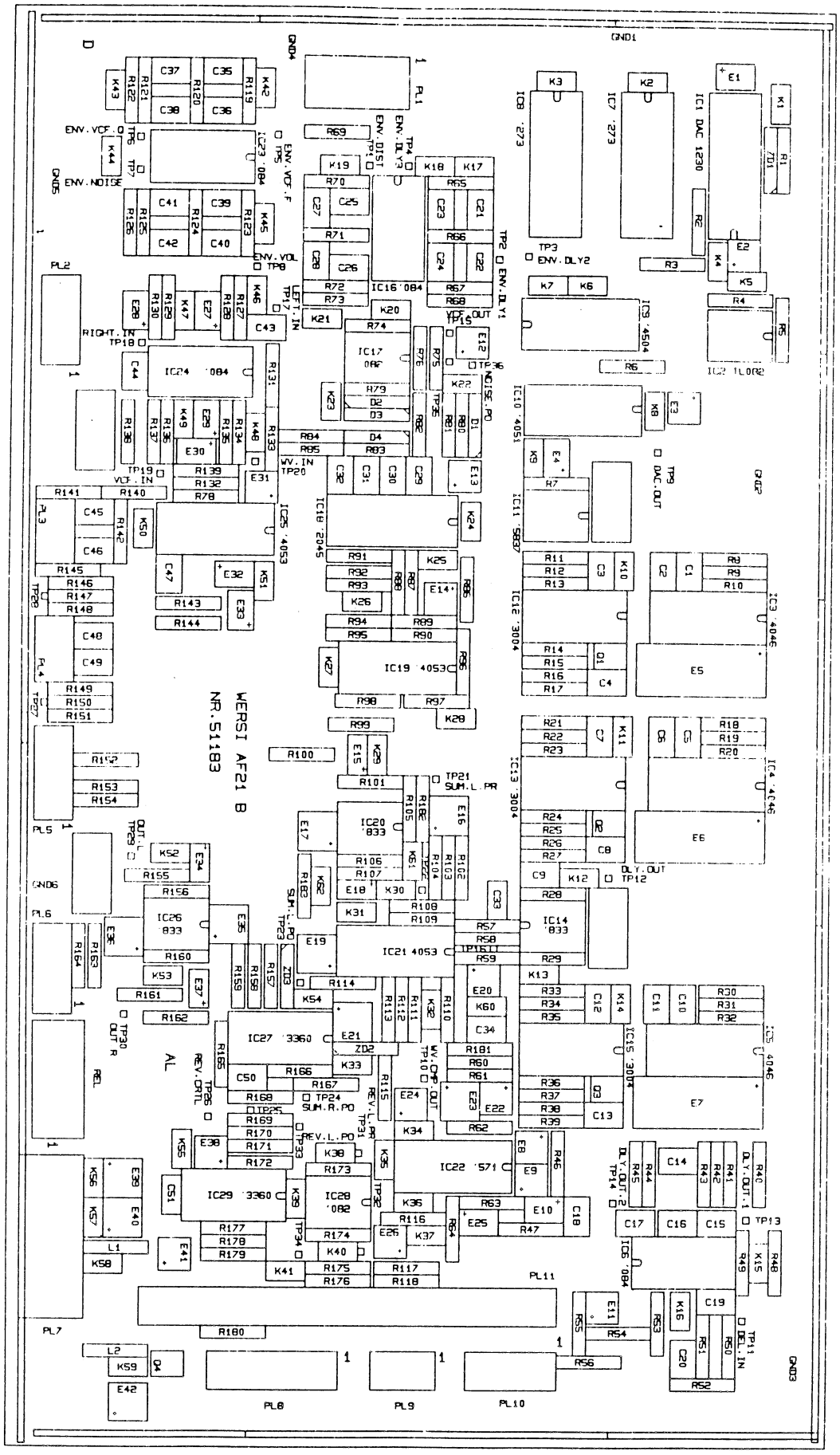


Fig. 32b: Component layout of PC board AF 21

J. Technical Description of PC Board DH 10

The input signal (plug 1, pin 5) travels through C 31 (4.7 nF) to the input of the IC 14 (NE 571, pin 6).

A dynamic compression and level restriction to max 5 V_{SS} (D 7, D 8) is obtained with IC 14a and IC 16a (TL 084). The following low pass filter (IC 16b, c, d) is used for filtering (4 kHz: about -60 dB).

The signal adjusted in this way in frequency response and dynamics for digitilization is kept at a constant amplitude with IC 13 (LF 398, sample and hold) for the necessary conversion time of the analog-digital converter (ADC 1210, IC 11).

IC 11 then converts the analog signal to a 12-bit code, which – divided into 2 bytes – switches through with IC 5 and IC 6 (74 LS 244) one after the other to CPU (IC 1, 68 B 09). The CPU is controlled by the programs stored in IC 2 (2-kbyte EPROM) (short and long reverb, fast and slow echo). The CPU shifts the digital information (data) into a memory (IC 7, 2 k x 8 RAM) – read out with a time offset – adds it to other data, restores it, etc.

This is repeated with the 12-bit code of the ADC until reverb times up to 4 sec are reached, with CPU and RAM operating at a width of 16 bytes. The finished signal (again 12 bits) is again broken down into 2 bytes and transmitted in 2 steps to the digital-analog converter (DAC 1230, IC 12), which generates an analog current corresponding to the digital value.

This current is converted with IC 15c (TL 084) to a voltage which, however, still contains amplitude jumps and undesired frequency components because of the prior digitilization.

In the subsequent low pass filter (IC 15a, b, d), the signal is smooth: the interference components are filtered out.

The above-described level rise and dynamic restriction of the input signal is eliminated with C 40 (33 nF) and IC 14b.

The output signal travels over Ju 1 to the output (6) or through the stereo-converter IC 17.

The switching of the various modes (short and long

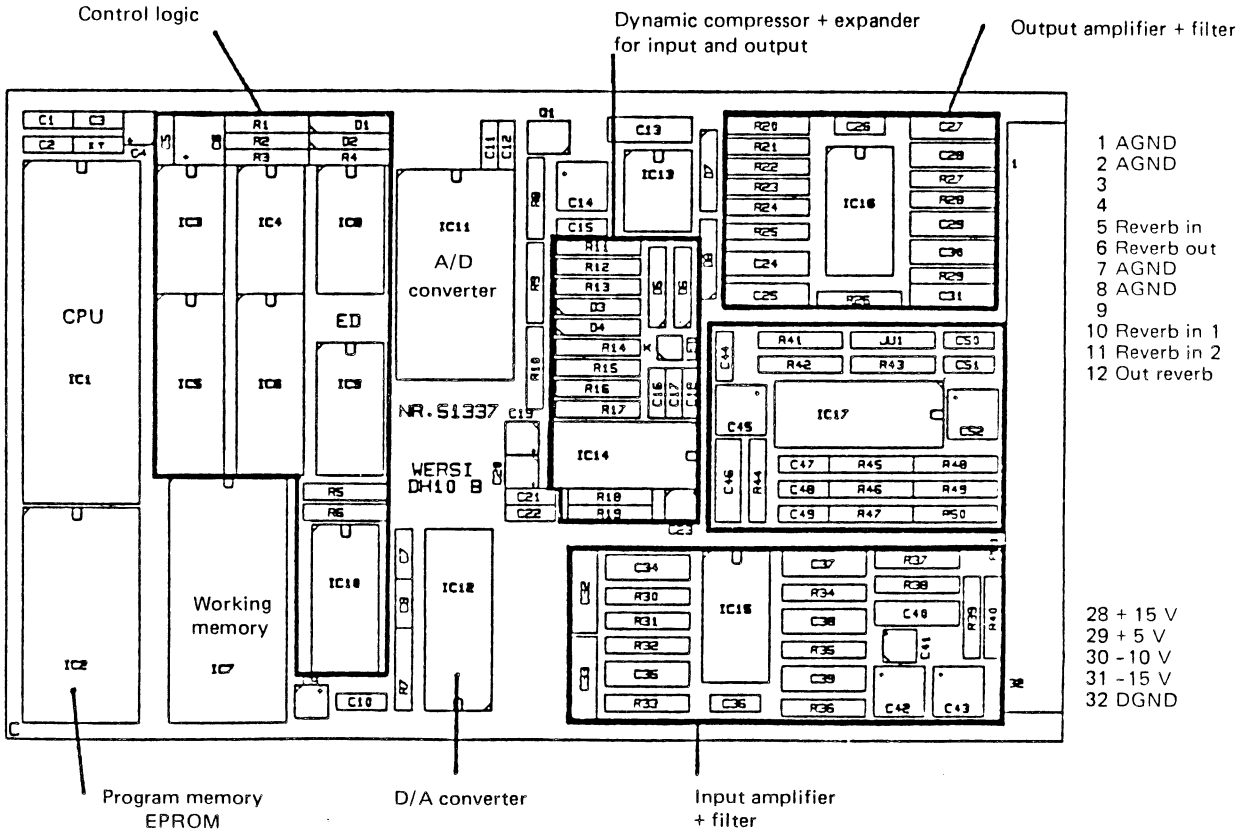


Fig. 33: Component layout of PC board DH 10

reverb, rapid and slow echo) is done via NMI of the CPU by voltage pulses to pin 12.

The running of the program (voltage at pin 10, 11) is activated with reset (CPU).

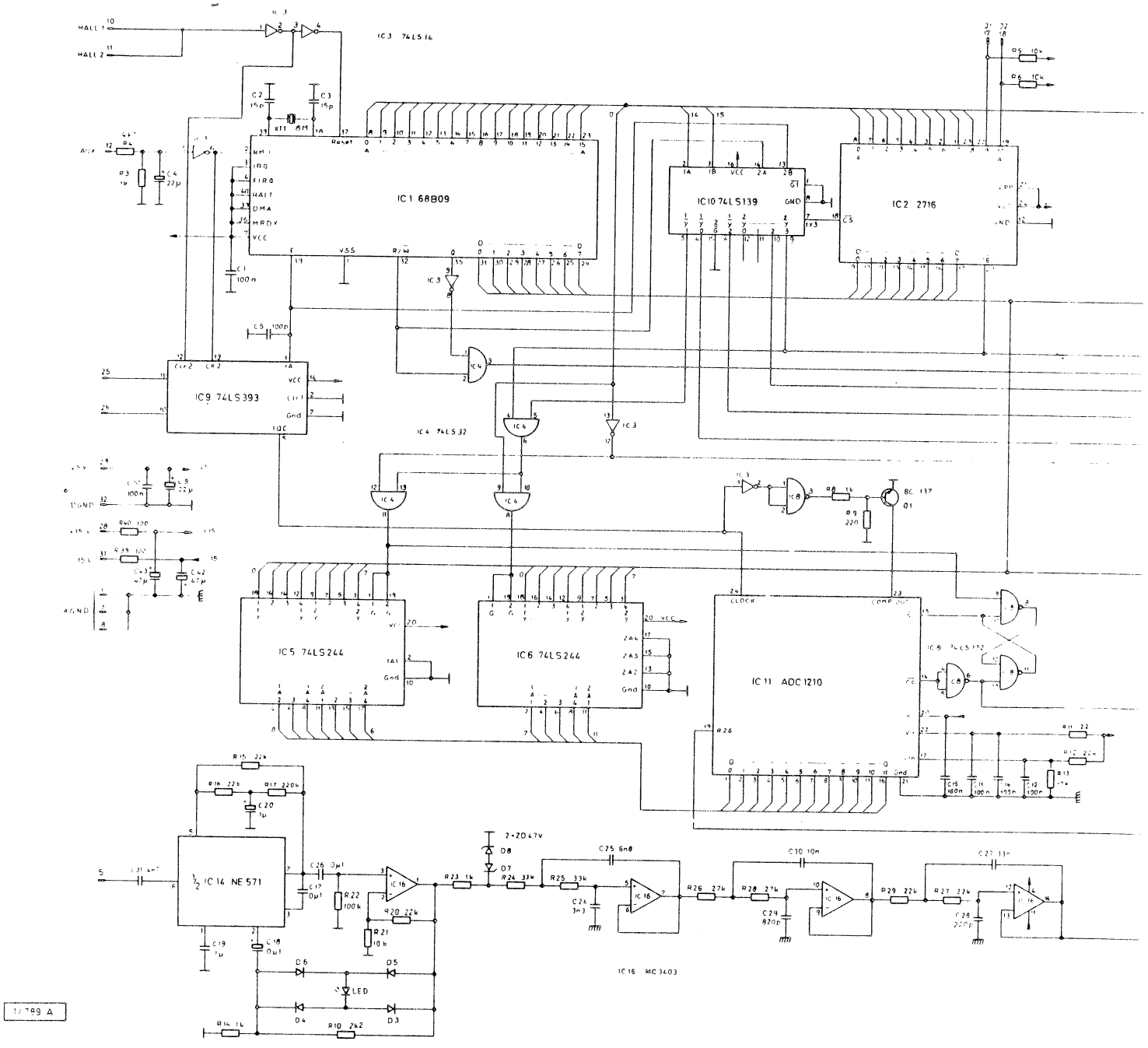
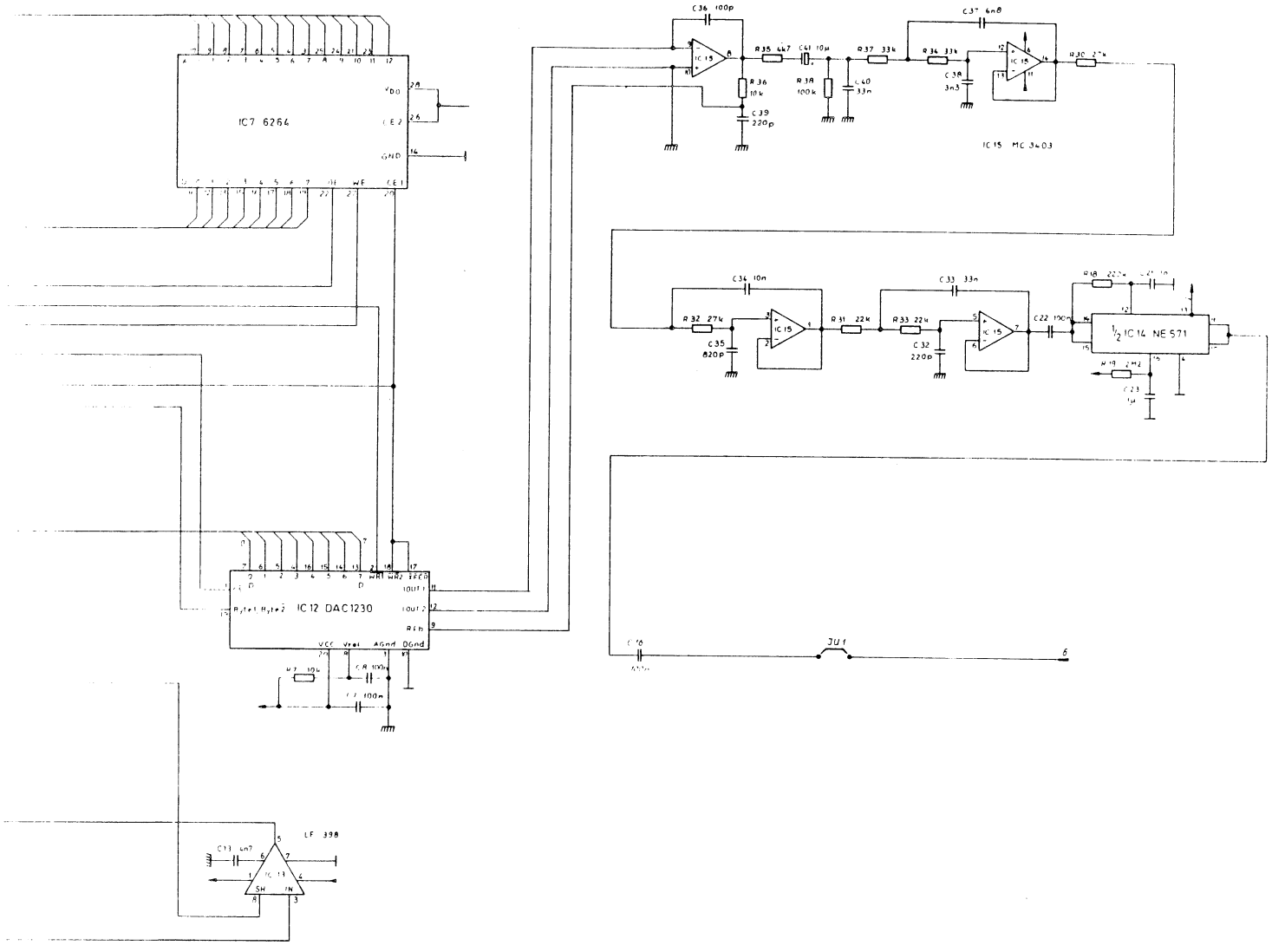


Fig. 34a: Circuit diagram of PC board DH 10 (mono, with AF 20)


IC7 6264
VDD
CE2
GND
WE
CE1
C36 100p
R35 4k7
C41 10µ
R37 33k
C37 6n8
R36 33k
R30 27k
R36 10k
C39 220p
R38 100k
C40 33n
C38 3n3
IC15 MC 3403
C34 10n
C33 33n
R32 27k
C35 820p
R31 22k
R33 22k
C32 220p
C22 100n
1/2 IC14 NE 571
C23 1µ
IC12 DAC1230
VCC
Vref
AGnd
DGnd
R7 10k
C8 100n
C7 100n
C16
JU1
LF 398
C13 4n7
IC13
SH
IN

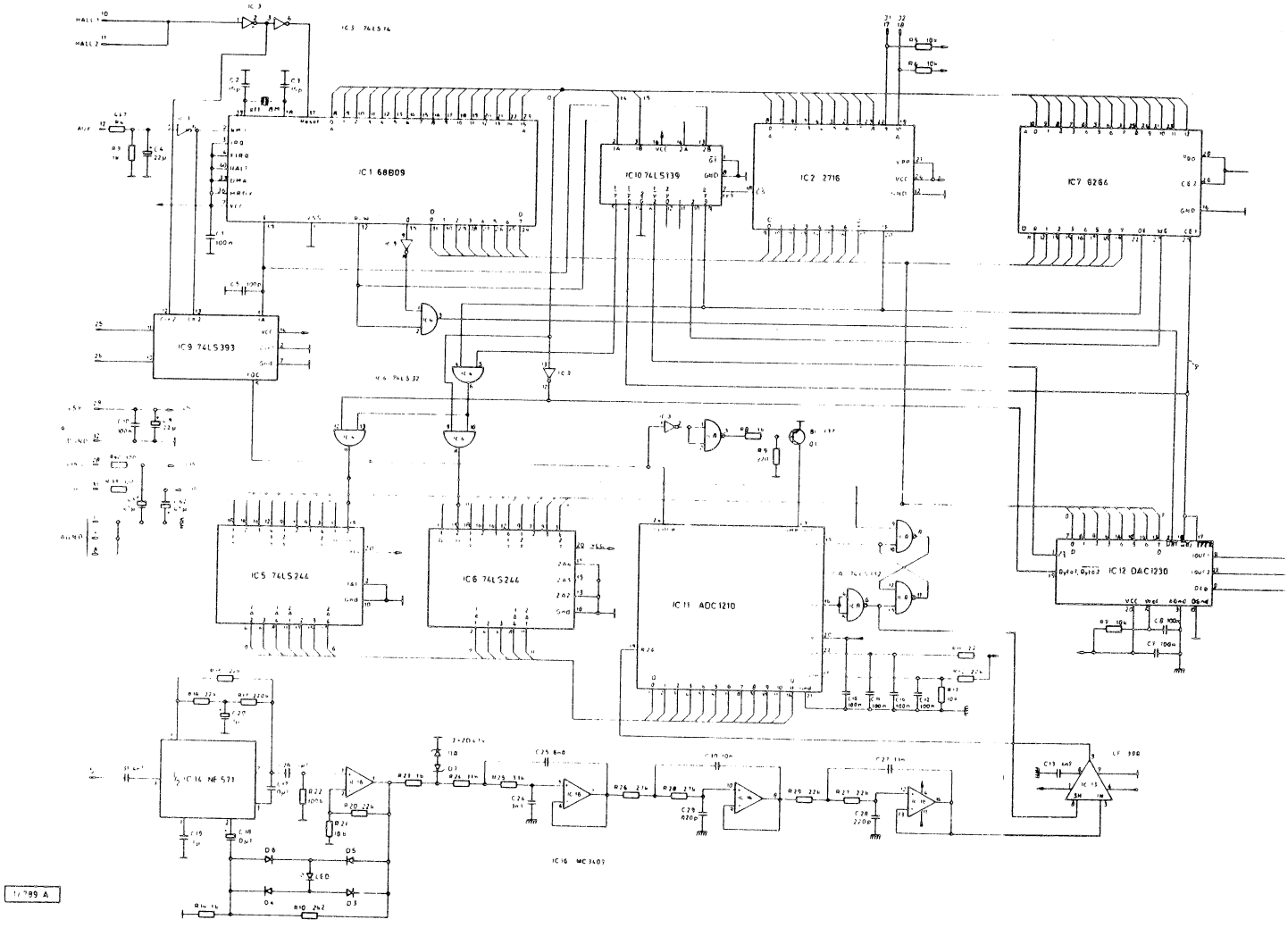
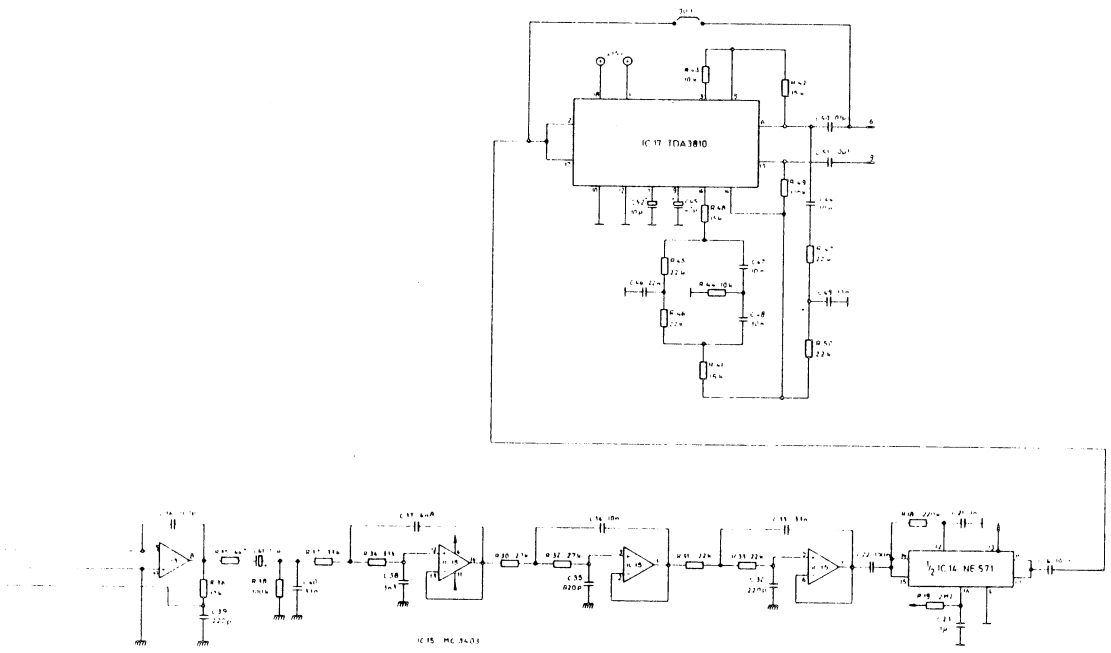


Fig. 34b: Circuit diagram of PC board DH 10 (stereo, with AF 21)


IC 17 TDA3810
½ IC 14 NE 571

K. Technical Description of PC Board CX 7 and CBM 29 (DX 10 only), Fig. 35

On PC Board CX 7, the microprocessor (IC 15) continuously monitors the master data bus via IC 26, from which it receives the instrument triggers. IC 15 then directs the readout of the memories (IC 20-22) which store the digitally recorded instrument sounds. The digital sounds are latched through IC 18 to IC 10 (Digital/Analog Converter). The output of IC 10 and IC 1 contains all the analog sounds but in multiplexed form. IC 9 demultiplexes the signals according to volume. The signals are summed together at IC 8 and demultiplexed by instrument at IC 5. After filtering by IC's 6 and 7 and summing by IC 4, final amplification and volume control occurs at IC 2 before being sent to AF 21 via PL 1.

CBM 29 operates in the same manner as CBM 31.

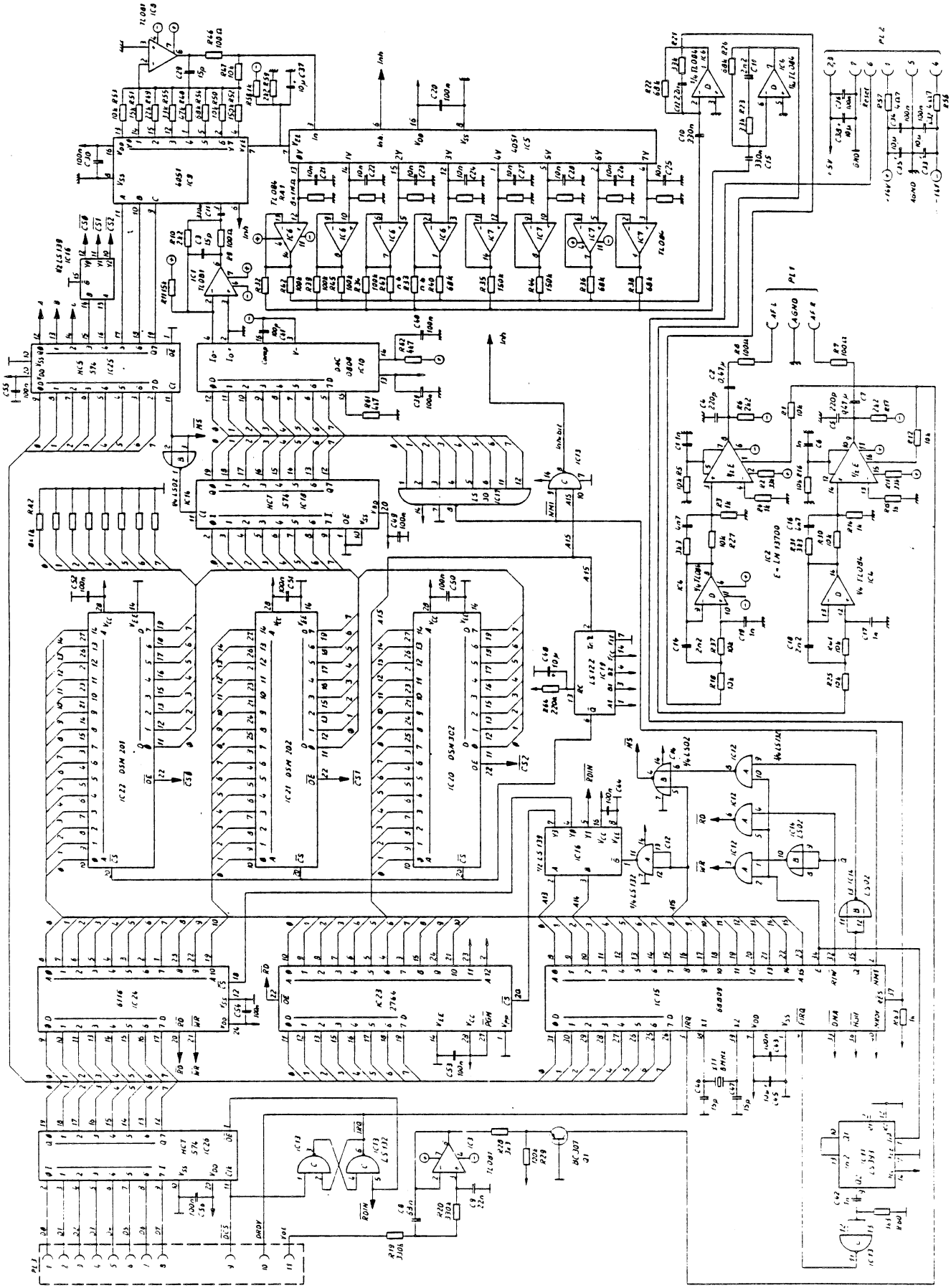


Fig. 35: Circuit diagram of PC board CX 7

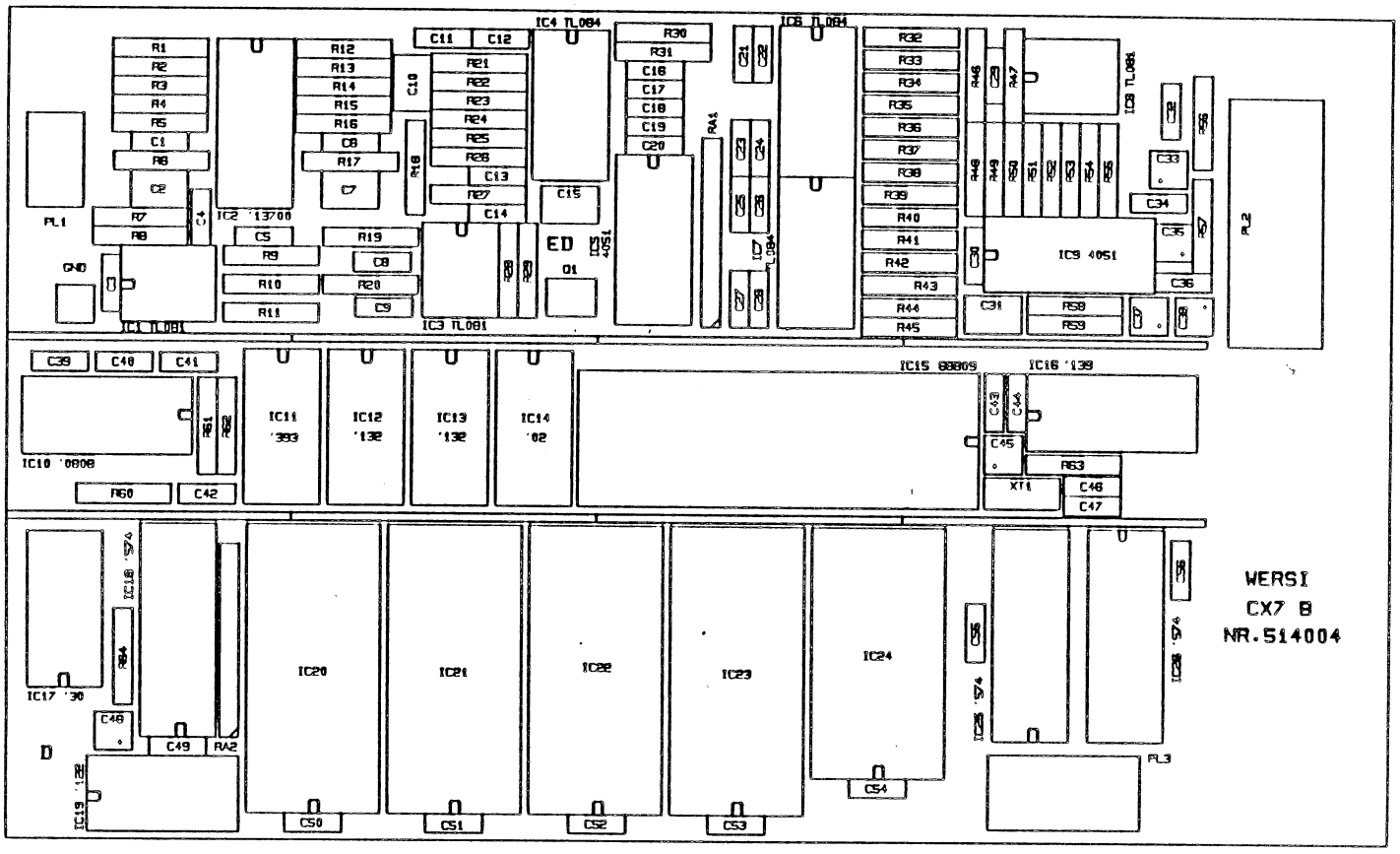


Fig. 36: Component layout of PC board CX 7

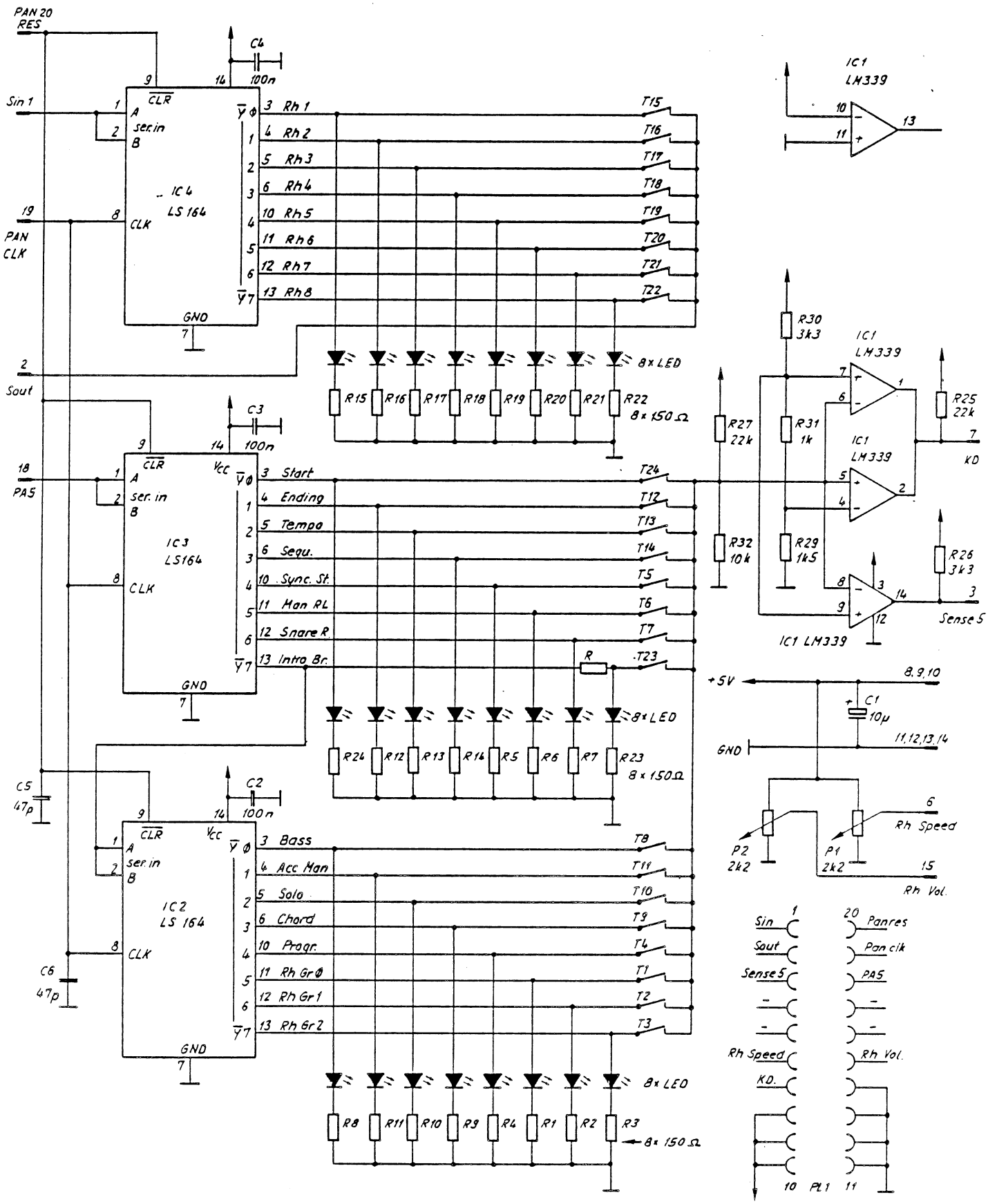


Fig. 37: Circuit diagram of PC board CBM 29

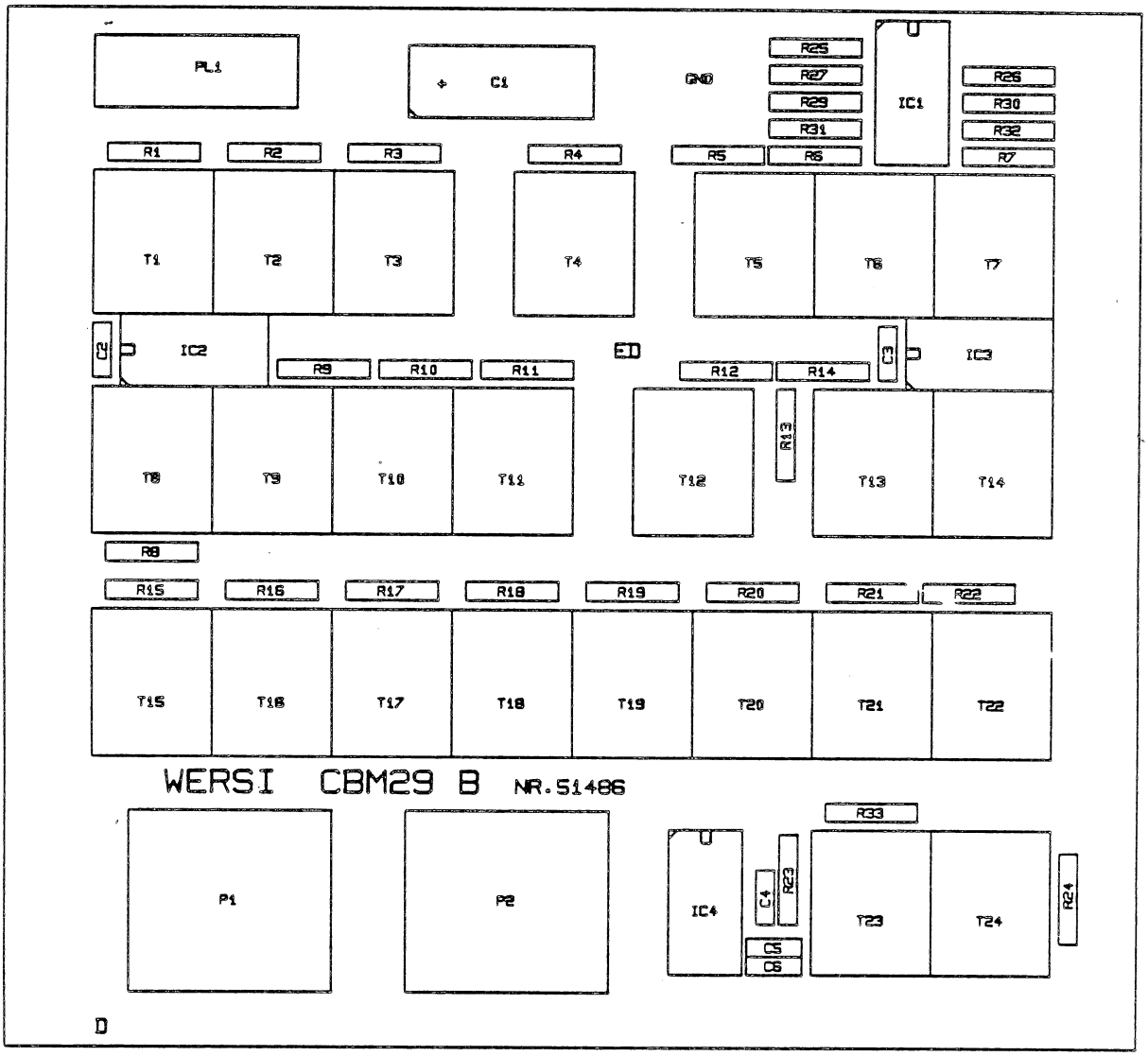


Fig. 38: Component layout of PC board CBM 29

L. PC Boards PA 102 and PA 104 (in OMEGA only)

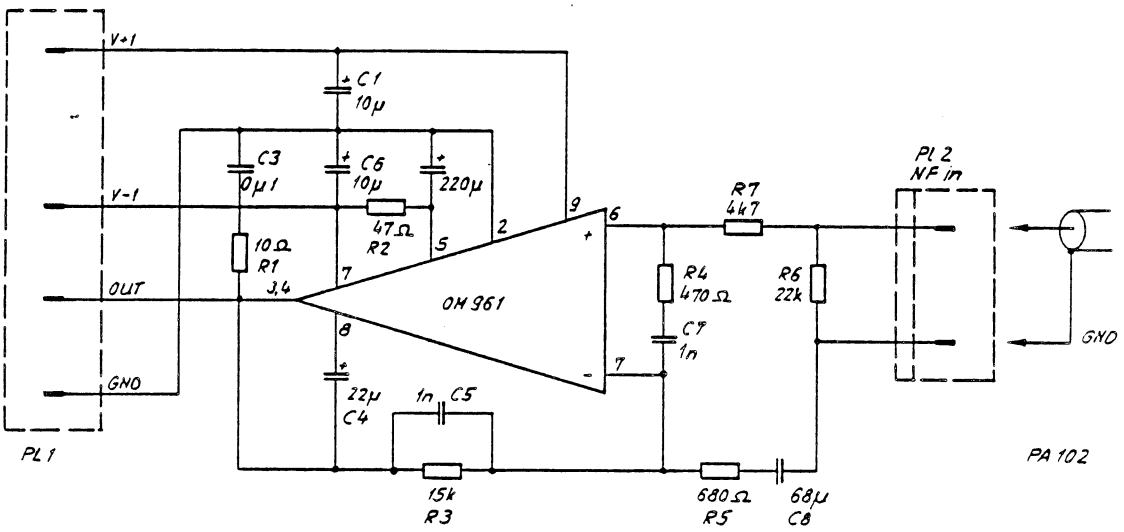


Fig. 39: Circuit diagram of PC board PA 102

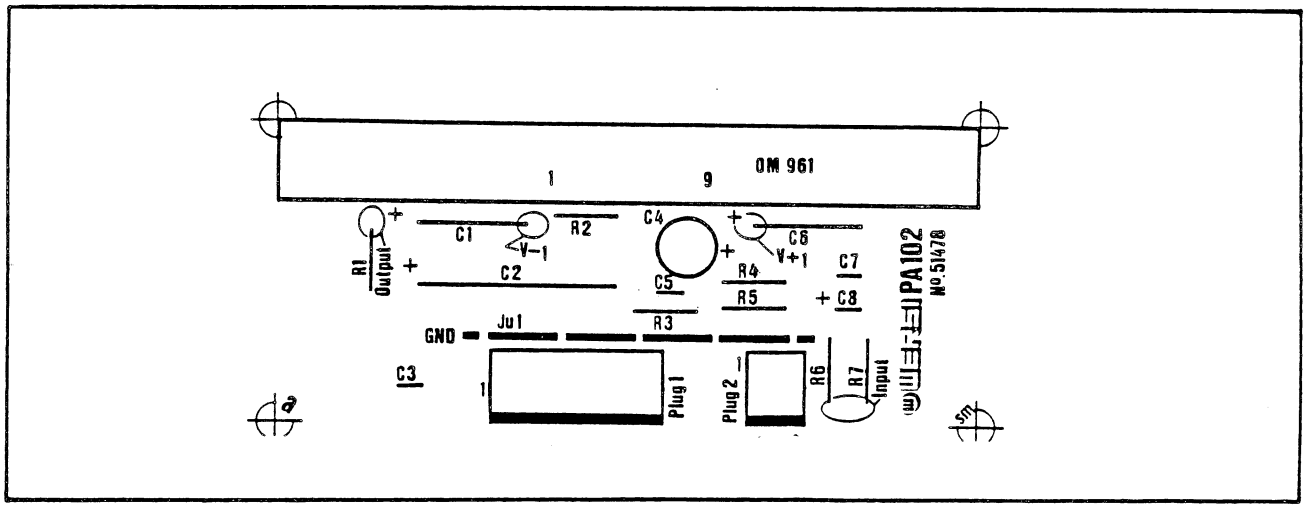


Fig. 40: Component layout PA 102.

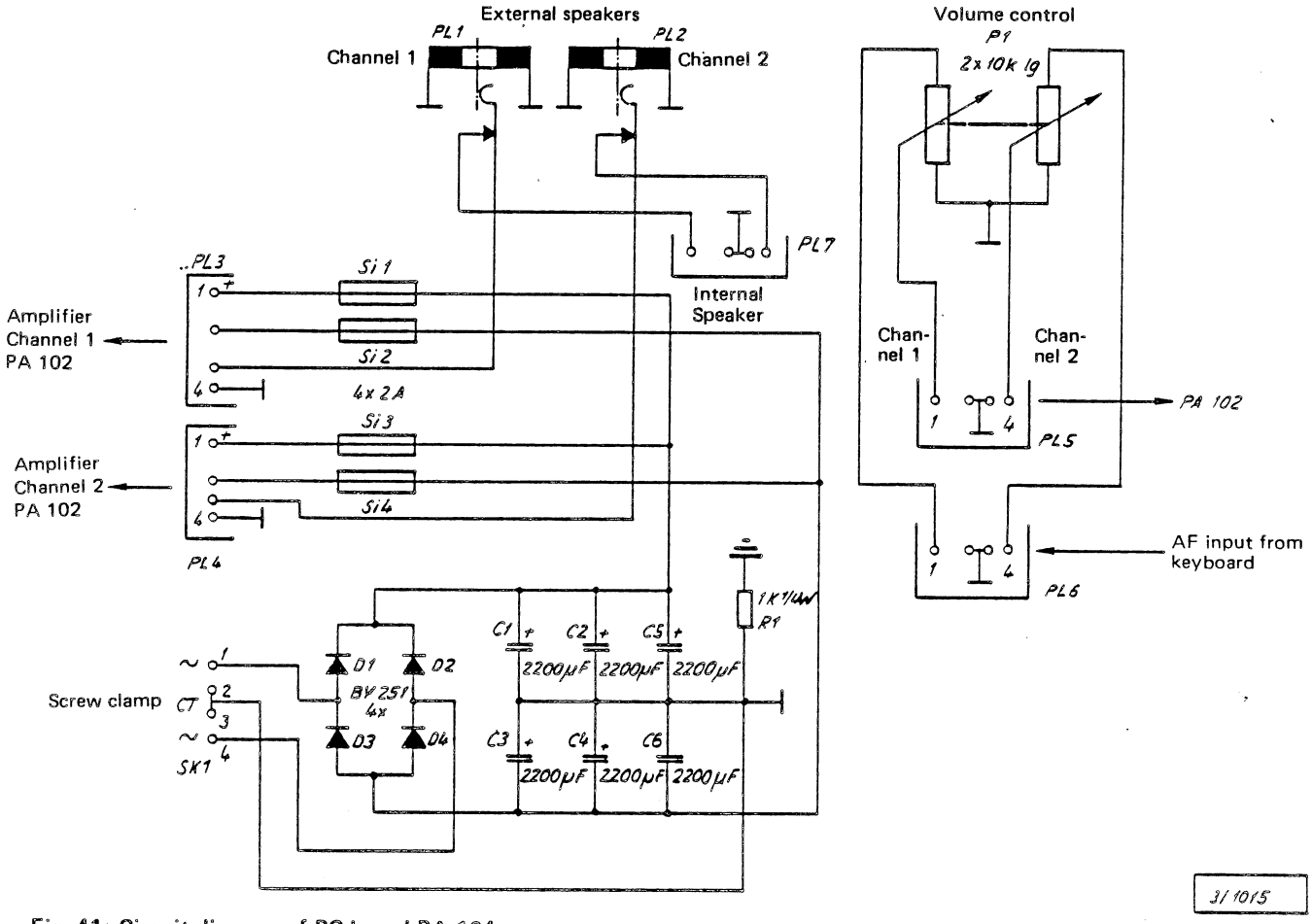


Fig. 41: Circuit diagram of PC board PA 104

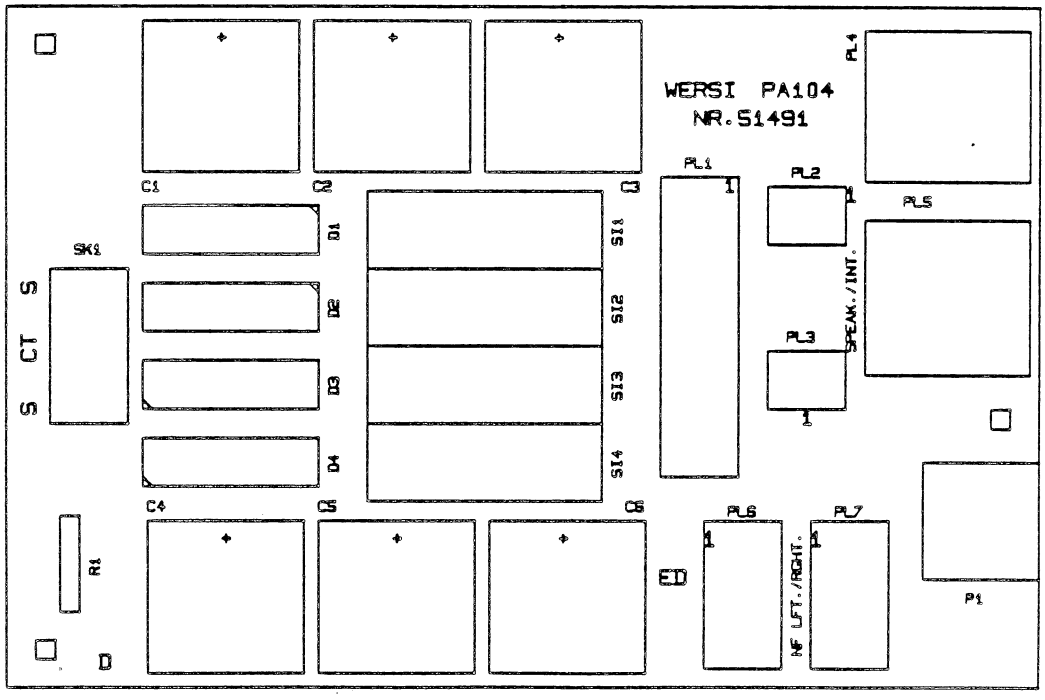


Fig. 42: Component layout PA 104

M. Note Concerning PC Board ME 2

PC board ME 2 – control panel of the Expander EX 10 – performs the same functions as PC board CBM 30, 31 and 36 of the OMEGA. The technical description for CBM 30 and 31 also applies to PC board ME 1.

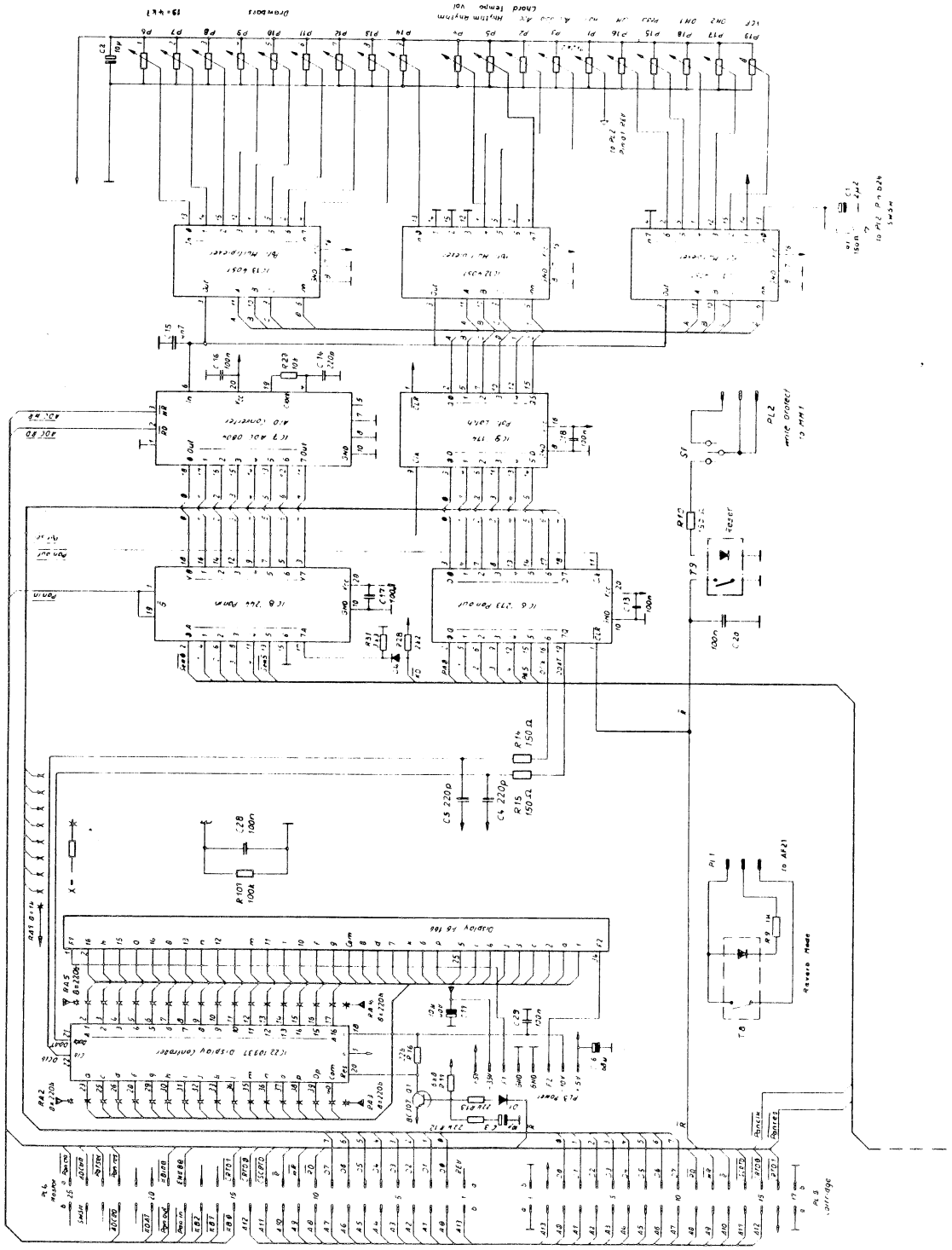
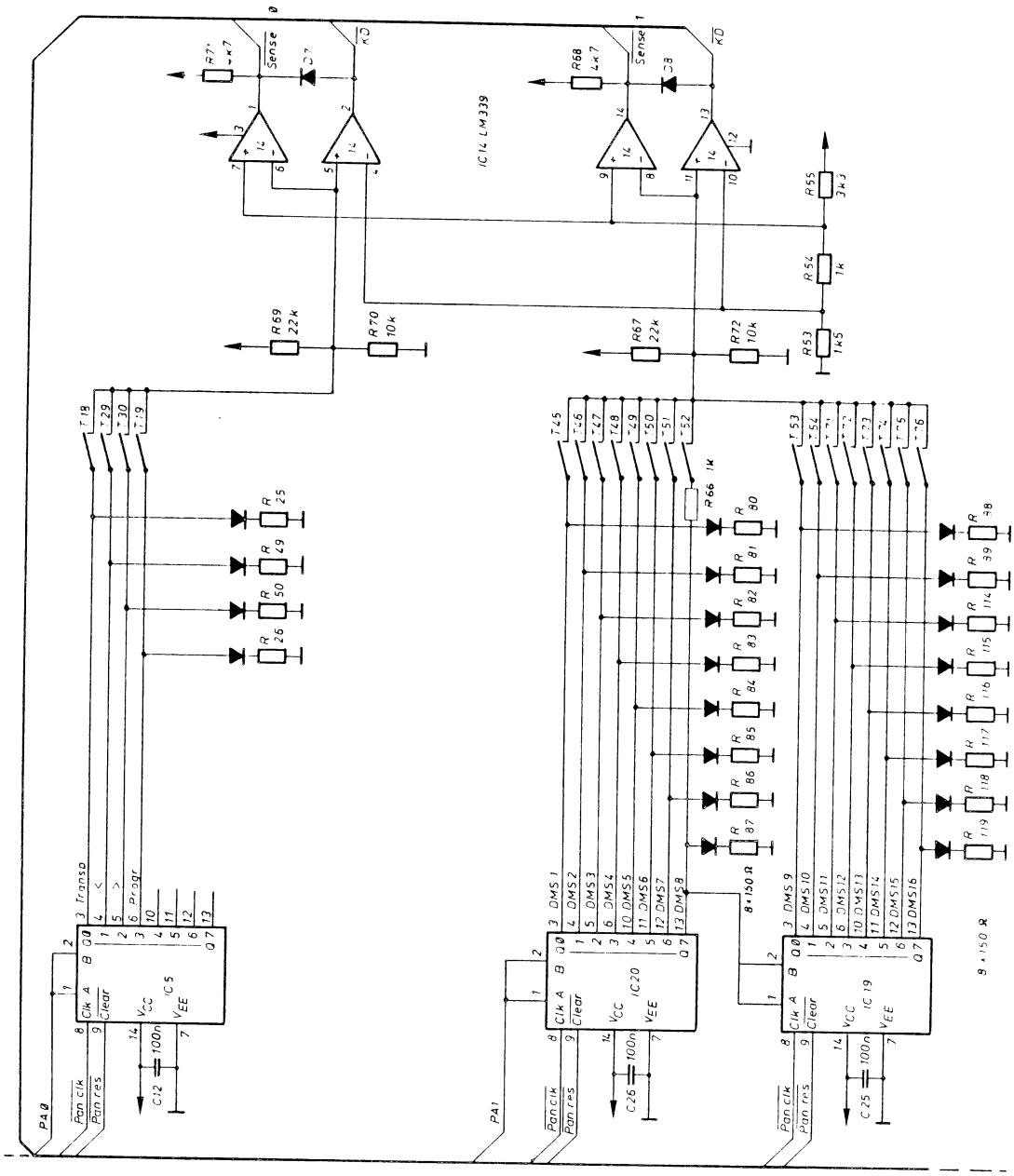
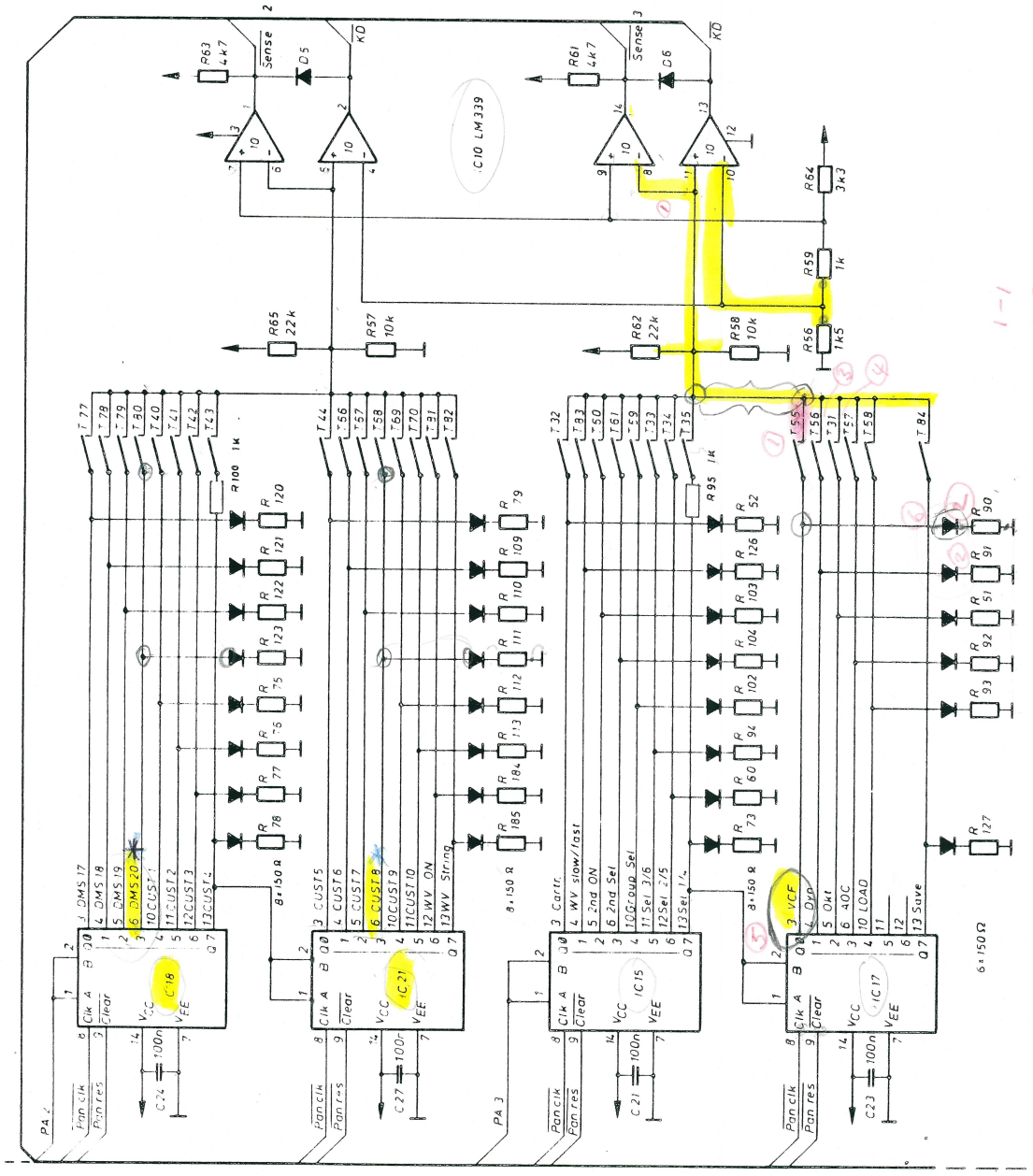
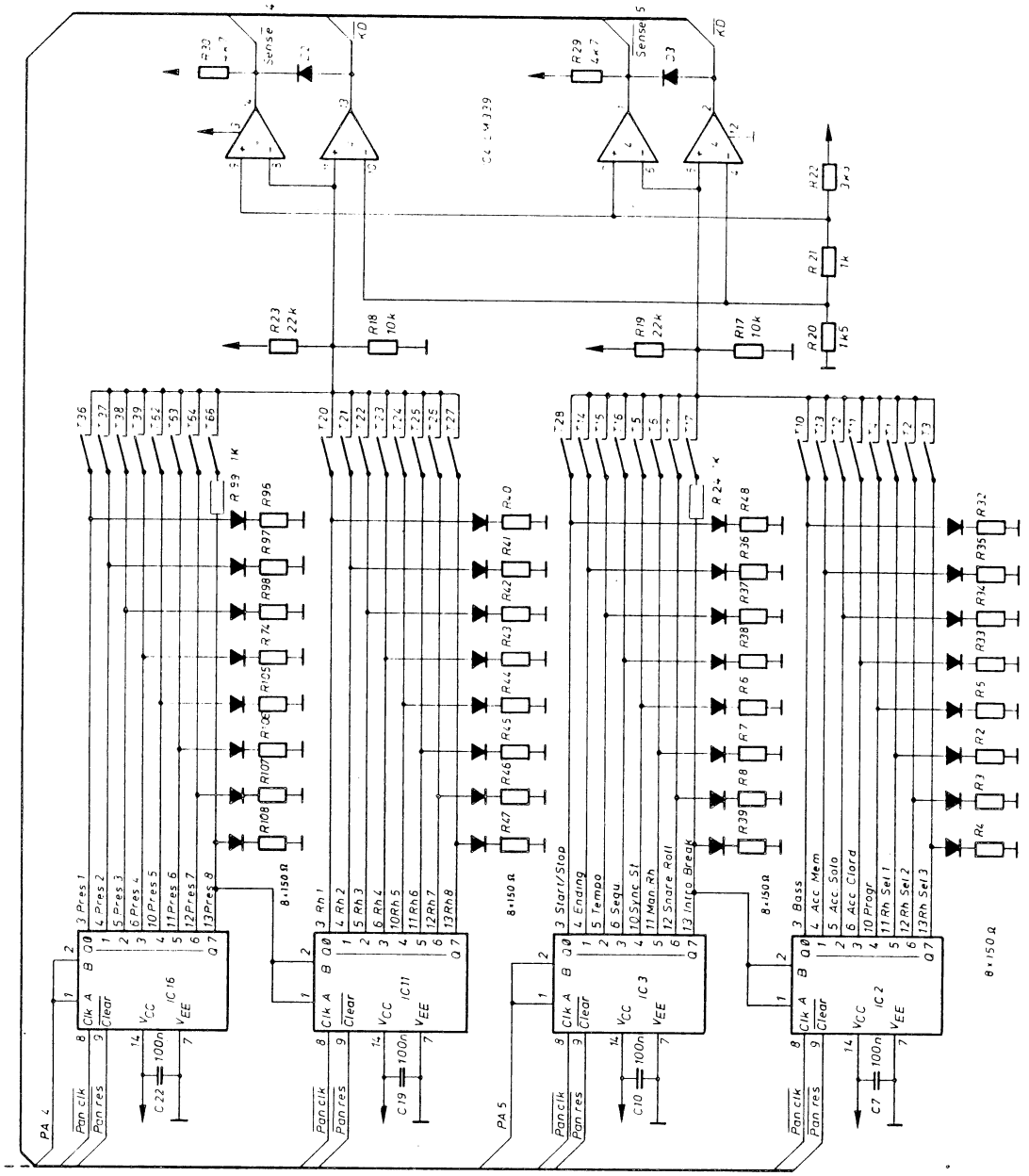


Fig. 43: Circuit diagram of PC board ME 2


IC14 LM339
Sense 0
Sense 1
R71 4k7
R68 4k7
R69 22k
R70 10k
R67 22k
R72 10k
R55 3k3
R54 1k
R53 1k5
R66 1k
8 x 150 Ω
8 x 150 Ω
3 Transp
4 <
5 >
6 Progr
10
11
12
13
DMS 1
DMS 2
DMS 3
DMS 4
DMS 5
DMS 6
DMS 7
DMS 8
DMS 9
DMS 10
DMS 11
DMS 12
DMS 13
DMS 14
DMS 15
DMS 16
Clk A
Clear
Q0
Q7
VCC
VEE
IC 5
IC20
IC 19
Pan clk
Pan res
C12 100n
C26 100n
C25 100n
P40
P41


IC10 LM339
Sense
KD
D5
D6
R63 4k7
R61 4k7
R64 3k3
R59 1k
R56 1k5
R65 22k
R57 10k
R62 22k
R58 10k
R100 1k
R95 1k
8 x 150 Ω
6 x 150 Ω
IC18
IC21
IC15
IC17
C24 100n
C27 100n
C21 100n
C23 100n
1 DMS 17
4 DMS 18
5 DMS 19
6 DMS 20
10 CUST 1
11 CUST 2
12 CUST 3
13 CUST 4
3 CUST 5
4 CUST 6
5 CUST 7
6 CUST 8
10 CUST 9
11 CUST 10
12 WV ON
13 WV String
3 Cartr.
4 WV slow/fast
5 2nd ON
6 2nd Sel
10 Coupl Sel
11 Sel 3/6
12 Sel 2/5
13 Sel 1/4
3 VCF
4 Oxp
5 Okt
6 40C
10 LOAD
13 Save
Clk A
Clear
VCC
VEE
Pan Clk
Pan res
PA 2
PA 3

* Bridged


Sense
+5
R23 22k
R18 10k
R19 22k
R17 10k
R20 1k5
R21 1k
R22
R99 1k
R24 1k
8 * 150 Ω
IC 16
IC 11
IC 3
IC 2
Clk A
Clear
Pan clk
Pan res
VCC
VEE
100n
PA 4
PA 5
3 Pres 1
4 Pres 2
5 Pres 3
6 Pres 4
10 Pres 5
11 Pres 6
12 Pres 7
13 Pres 8
3 Rh 1
4 Rh 2
5 Rh 3
6 Rh 4
10 Rh 5
11 Rh 6
12 Rh 7
13 Rh 8
3 Start/Stop
4 Ending
5 Tempo
6 Sequ
10 Sync St
11 Man Rh
12 Snare Roll
13 Intro Break
3 Bass
4 Acc Mem
5 Acc Solo
6 Acc Clord
10 Progr
11 Rh Sel 1
12 Rh Sel 2
13 Rh Sel 3

List of all Abbreviations Used

Name	Technical Description	Bus	PC Board
ACIRQ	ACIA IRQ	Control	MM 1: IC 7, 14
ADAC	ANALOG DAC Select	Select	MM 1: IC 12, PL 4, AF 20, IC 25
ADCRD	ADC Read Select	Select	MM 1: IC 8, PL 1; CB 30; IC 8
ADCWR	ADC Write Select	Select	MM 1: IC 15, PL 1; CB 30; IC 8
AGND	Analog Ground		
AMOND	Modulations Byte to AF 20	Select	MM 1: IC 49, PL 4; AF 20; IC 22
AROUT	Routing Byte to AF 20	Select	MM 1: IC 49, PL 4; AF 20; IC 23
AS	Address Strobe (Slave)	Slave	Slaves SL-M2; MM 1; IC 29
B 0...B 7	Slave Address/Data Bus	Slave	MM 1: IC 29...31, Slaves SL-M2
CRAR	Clear Ram Access (Master)	Select	MM 1: IC 15, 34
CRES	Co-processor RESET	Control	MM 1: IC 17, 42
CRTDØ	Cartridge Coding Ø	Control	MM 1: PL 1, IC 10; CB 30; CB 35
CRTD 1	Cartridge Coding 1	Control	MM 1: PL 1, IC 10; CB 30; CB 35
CR/W	Co-processor R/W	Control	MM 1: IC 42, 23, 27, 38, 40
CSCRTD	Cartridge Select	Select	MM 1: IC 9, PL 1; CB 30; CB 35
DCLK	Display Clock	Panout	CB 30: IC 10, 6
DDAT	Display Data	Panout	CB 30: IC 10, 6
DCS	Drum Select (only DX 10)	Select	MM 1: IC 15, PL 5
DGND	Digital Ground		
DRDY	Drum Ready (only DX 10)	Select	MM 1: PL 5, IC 10
DRV	Drum Volume (only DX 10)	Control	MM 1: PL 1, 5
DS	Data Strobe (Slave)	Slave	Slaves SL-M2; MM 1; IC 31, 33
E	System Clock 2 MHz	Control	MM 1: IC 18,
ECLK	Envelope Clock (1...20)	Slave	MM 1: IC 41; MME 1; IC 5, Slaves
ENKBQ	Enable Keyboard Interrupt	Control	MM 1: IC 11, PL 1; CB 30; KD 10, IC 1
EXSLAØ	Exponent for Slave Pitch	Slave	MM 1: IC 17; Slaves SL-M2
EXSLA 1	Exponent for Slave Pitch	Slave	MM 1: IC 17; Slaves SL-M2
EXT	Ext. Select (not used)	Select	MM 1: IC 15, PL 1
FIRQ	Fast Interrupt 68 B 09	Control	MM 1: IC 14, 18
GND	Ground		
IO	Input/Output Select Region	Select	MM 1: IC 14, 6, 7, 12
IRQ	Interrupt 68 B 09	Control	MM 1: IC 14, 18
KBIRQ	Keyboard Interrupt	Control	KD 10: IC 1; CB 30; MM 1; IC 10, 14
KD	Key-Down (Panel Switch)	Panin	CB 31: IC 1, 7; CB 30; PL 3, 4, IC 7
KDAT	Keyboard Data	Address	MM 1: IC 12, 8, PL 1; CB 30; IC 9
KEYBØ	Keyboard Select Ø (Sound No.)	Select	MM 1: IC 8, PL 1; CB 30; KD 10; IC 3
KEYB1	Keyboard Select 1 (Dynamics)	Select	MM 1: IC 8, PL 1; CB 30; KD 10; IC 2
KEYB2	Keyboard Select 2 (free)	Select	MM 1: IC 8, PL 1; CB 30; PL 5
MUXOUT	Multiplex Output Envelope		MM 1: R 14, IC 27, 44, 45, PL 25; MME 1
PA 0...5	Peripheral Address (6 bits)	Panout	CB 30: IC 10, PL 3, 4, 5; CB 31
PANCLK	Panel Clock	Select	MM 1: IC 15, PL 1; CB 30; CB 31
PANIN	Panel in Port Select	Select	MM 1: IC 8, PL 1; CB 30; IC 7
PANOUT	Panel Out Latch Select	Select	MM 1: IC 8, PL 1; CB 30; IC 10
PANRES	Panel Reset	Select	MM 1: IC 15, PL 1; CB 30; CB 31
POTSEL	Potentiometer Select Latch	Select	MM 1: IC 15, PL 1; CB 30; IC 2
PROM	Program ROM Select	Select	MM 1: IC 35, 3
Q	System Clock 68 B 09	Control	MM 1: IC 18
QVECT	Interrupt Vector	Select	MM 1: IC 12, 10

Name	Technical Description	Bus	PC Board
R	Reset	Control	PS 20; MM 1; CB 30; AF 20
RAUD	RAM Access Update (Slave Start)	Slave	MM 1: IC 49, 50; MME: IC 4; Slaves
RARC	RAM Access Ready & Clear	Slave	MM 1: IC 33, 34; Slaves SL-M2
RD	Memory Read (Coupled with E)	Control	MM 1: IC 9,
REV	Reverb	Control	MM 1: PL 1, 4
RxD	ACIA Receiver data (MIDI In)	Control	MM 1: IC 7, PL 2
R/W	Read/Write 68 B 09	Control	MM 1: IC 18, 6, 9, 18, 43
SLIRQ	Slave Interrupt	Control	MM 1: IC 34, 10, 14
SEN	= SENSE		CB 30: PL 3, 4, IC 7
SENSE	Switch Identification Group	Panin	CB 31: IC 1, 7; CB 30; PL 3, 4, IC 7
SIN	Serial IN (Group 3)		CB 31: IC 7; CB 30; PL 3, IC 3
SLRAM	Slave RAM Select	Select	MM 1: IC 9, 30, 33, R 20
SLRAMB	Slave RAM Bank Latch Select	Select	MM 1: IC 8, 17
SLRWR	Slave RAM Write	Slave	MM 1: IC 33, 31
SOUT	Serial OUT (Group 3)		CB 31: IC 6, CB 30; PL 3, Switch
SWELL	Swell Pedal (Volume Pedal)	Control	CB 32; MM 1: PL 2, 1; CB 30; IC 1
SWØ	Switch Ø (Volume Pedal)	Control	CB 32; MM 1; PL 2, IC 10
SW1	Switch 1 (+VCF Calibration)	Control	CB 32; AF 20: Q 7; MM 1; PL 2, IC 10
TIRQ	Timer Interrupt	Control	MM 1: IC 6, 10, 14
TxD	ACIA Transmit Data (MIDI Out)	Control	MM 1: IC 7, PL 2
VCS	Volume Control Select (free)	Select	MM 1: IC 49, PL 5
VRAMB	Voice RAM Bank Latch Select	Select	MM 1: IC 49, 11
VRAME	Voice RAM Enable (Bank Select)	Select	MM 1: IC 11, 13
VROME	Voice ROM Enable (Bank Select)	Select	MM 1: IC 11, 9
WR	Memory Write (Coupled with E)	Control	MM 1: IC 13,
0. . .7	Data Lines 0. . .7	Data	MM 1: IC 16,
0. . .15	Address Lines 0. . .15	Address	MM 1: IC 18, 19,
00, 08, 10	RAUD Group Selects	Address	MM 1: IC 12, 49, 50, PL 25; MME 1: IC 4
18, 20	Vor-decoder, Addresses, 8 bytes Each	Address	MM 1: IC 12, 15, 13
12 M 1	12 MHz Clock for Slave 1. . .12	Slave	MM 1: IC 33; Slaves SL-M2
12 M 2	12 MHz Clock Inverted 1. . .12	Slave	MM 1: IC 33; Slaves SL-M2
12 ME 1	12 MHz Clock for Slave 13. . .20	Slave	MM 1: IC 33; Slaves SL-M2
12 ME 2	12 MHz Clock Inverted 13. . .20	Slave	MM 1: IC 33; Slaves SL-M2
0000	Co-processor Address Region	Select	MM 1: IC 40, 24, 23, 43
2000	Work RAM Select 2000. . .3fff	Select	MM 1: IC 25, 4
4000	Voice RAM (Bank) 4000. . .5fff	Select	MM 1: IC 25, 43, 13
6000	V Bank RAM (Bank) 5000. . .7fff	Select	MM 1: IC 25, 43, 13
4/6000	V ROM Cartr. (Bank) 4000. . .7fff	Select	MM 1: IC 43, 9

MEMORY MAP (Master Processor)

Address Regions	Name	Length (Bytes)
0000...00ff	Slave RAM	256
0100...01ff	Input/Output	256
0200...1fff	Co-processor RAM	8 kB-512
2000...3fff	Work Ram	8 kB
4000...7fff	Voice Bank Region	16 kB
8000...ffff	Program ROM	32 kB

MEMORY MAP (Co-Processor)

Address Regions	Name	Length (Bytes)
0000...3fff	(Not allowed)	–
4000...5fff	MUX Latch	1
6000...7fff	ECLK Strobes	20
8000...9fff	Envelopes DAC	2
a000...dfff	(Not allowed)	–
e000...ffff	Slave RAM	8 kB

STARTING THE DIGITAL ELECTRONICS (PC Board MM 1, CBM 30/31, AF or 21)

Since the location of errors in the digital region requires in-depth knowledge about computer hardware, some check-ups were written into the software to simplify trouble shooting.

Each time the unit is switched on, after resetting the hardware, the main CPU tests some functional groups. This is done before or during the blink mode of the DX 10/EX 10.

First the working RAM IC 4 is tested for writability and readability; then the same test is done with the dual-port co-processor RAM IC 26.

After this test is passed, the first information is written into the display, and all switch groups are switched on alternately between the top and bottom row. The VCF on the analog PC board is then calibrated. To do this, the clock cycle of the VCF oscillator is switched to the foot pedal input and the CPU measures the frequency. When the latter is finished, the other rows are switched on and the measuring process started again.

If a defect occurs during these pre-tests, it must be determined on the basis of the LED pattern or the display.

1. If all LEDs are out and only the switch "Transposer ON" of the matrix is on, there is a defect in the working RAM.
2. If only the switches "Transposer on" and "down" light up, the defect is in the region of the co-processor RAM (IC 26, 36, 20. . .23).
3. The switch rows remain on, alternately top and bottom, without alternating blinking if no clock signal is coming from PC board AF 20. (PC board AF 20 must be connected!). The display included: "VCF – ADJUST". (This paragraph does not apply if your unit is equipped with an AF 21 PC board.)

If all tests are passed and the row of switches blink, any switch may be depressed.

Test phase 1 is then interrupted and the main processor initializes its working memory with the latest state of a preset. A "check sum" is also tested, which is recalculated during each programming of CV or a preset.

If the test is negative, the data in the Voice RAM or voice bank RAM are invlaid and the CPU attempts to write in these RAMs the standard presets on CVs. This is indicated in the display by: "CV-RAM-verify". If the RAMs are not present or if the write-protect switch is on, no initialization can occur, and the CPU recognizes no preset and Ø CVs. This means that in this initialization phase, the write-protect switch must be off.

After these procedures the instrument is ready to play.

1) VCF Switch on ME 2 Does not Blink During Self check.

2) VCF Switch Lights When any Switch on ME 2 is Pushed & Stays Lit All The Time

3) Checked out ME-2 Switch works changed out IC's on ME-2 Had No Effect.

4) Does EX10 EF 20 Bd work with the EX10 Coin distribution.

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